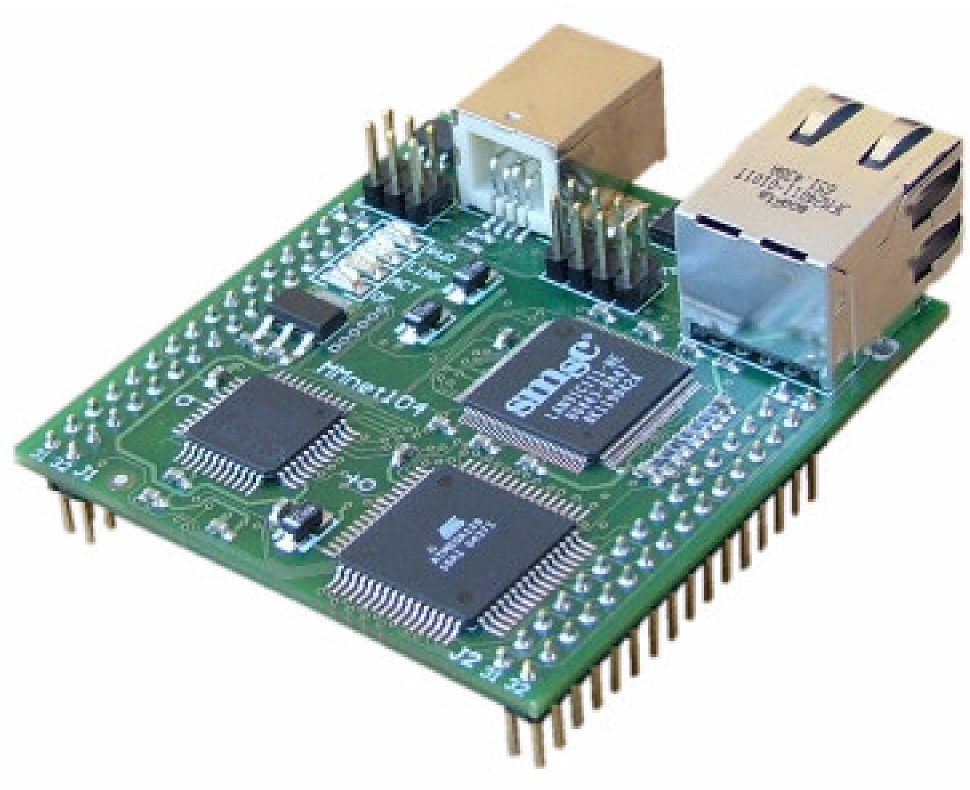


MMnet104 Ethernet Minimodule

User's Manual

REV 0.9

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Many ideas one solution

Contents

Introduction

Thank you very much for having bought our minimodule **MMnet104**. It was created with the idea of facilitating the communication of microprocessor systems through the Internet/Ethernet networks.

The heart of the module is the RISC Atmega128 microcontroller with 128kB of program memory and 128kB of (external) RAM memory, co-operating with the Ethernet RTL8018AS controller (100BaseTX). The memory controller built around a programmable CPLD device manages the address space of the microcontroller, generates address strobe/selection signals used during extension of the server by external I/O units, and serves the banking of RAM memory. The minimodule has an 8 MB DataFlash serial memory for storage of WWW pages and of any files e.g. with measurement data. The memory is connected to a fast SPI bus with 8 Mb/s transmission speed. The MMnet104 has been equipped with a RTC clock built around the DS1307 device, connected to the I2C bus. Together with the RTC circuit goes a socket for a lithium battery providing many guaranteed years of uninterrupted clock operation.

MMnet104 operates under real-time control **RTOS** allowing to build applications with the use of pseudo-concurrency in which different tasks are started and executed in the form of separate threads. This permits an easy construction of applications which require parallel execution of several tasks, for example servicing the TCP/IP stack and realizing the algorithm of control of an industrial process. The RTOS system has an extended interface for handling peripheral equipment, thanks to which the communication with them occurs via drivers registered in the system. The system has drivers for the Ethernet controller, serial ports, the 1-Wire bus, the DS 1820 thermometer, LCD display RTC clock and DataFlash memory. The kernel of the RTOS system and the TCP/IP stack together with implemented DHCP, UDP, ICMP, SMTP protocols and HTTP with simple CGI-s were compiled to libraries.

The system incorporates a series of demonstration applications (WWW server, FTP, Telnet, TCP client, TCP server, temperature monitoring and control, applications in the RTOS system) which are basing on completed functions present in the IP stack and RTOS operating system libraries. Attached libraries permit independent experiments (e.g. creation of web pages using the CGI technique without penetrating the lower layers of the IP stack and the RTOS operating system).

The **MMnet104** is delivered loaded with the WWW Server application and WWW demonstration pages with examples of using CGI and Flash. The configuration of the server (MAC address, IP, gateway, change of WWW page) can be effected remotely through serial RS232 or FTP ports.

Sources in C-language and ready libraries are attached to the server; they can be used to realize one's own projects. To modify and compile, the free C-compile GCC or C-compiler from ImageCraft can be put into use.

We wish you nothing but success and a lot of satisfaction in designing and developing new electronic equipment based on the MMnet104 minimodule.

Applications

The **MMnet104** minimodule can be used as a design base for electronic circuits co-operating from the Ethernet/Internet network, covering the following areas of interest:

- Industrial remote controlling and monitoring systems
- Telemetry
- Intelligent buildings
- Alarm systems
- Weather stations and environment monitoring
- Medical electronics
- Heating and air-conditioning systems
- Telecommunication
- Road traffic monitoring
- Remote data logging
- Home automation

The **MMnet104** minimodule can be also used in didactic workshops of information and electronic schools, illustrating the aspects of co-operation of electronic circuits from the Ethernet/Internet network, as well as be used to construct thesis circuits.

Features

- Fast RISC microcontroller ATmega128 with up to 16 MIPS throughput
- Ethernet controller IEEE 802.3 10/100Mb/s
- Onboard RJ45 connector with integrated magnetics and LED diodes
- Onboard USB interface (device) with USB-B connector
- 128kB of in circuit programmable FLASH program memory
- 128KB of RAM memory
- 4kB of EEPROM memory
- Serial DataFlash memory 32 or 64Mbit (4 or 8MBytes) (1)
- Flexible memory controller, allowing suit address space to application requirements
- I2C Real Time Clock and battery socket (1)
- Reliable reset circuit
- Crystal resonator 14.7456 or 16 MHz
- Crystal resonators 32.768 Hz for RTC and MCU internal timer/counter
- 4 LED diodes indicating: power, LAN activity, DataFlash activity
- Fully SMD made on 4-layer PCB
- 2 x 32 terminals with 0.1" (2.54mm) pitch fitting every prototype board
- Available free operating system with TCP/IP stack supporting many protocols
- Available evaluation board and sample applications
- Small dimensions: 56mm x 59mm

Remarks: 1. Assembled in dependence on the MMnet104 version

2 Construction of the module

Block diagram

The block diagram of the MMnet104 minimodule is shown in the drawing:

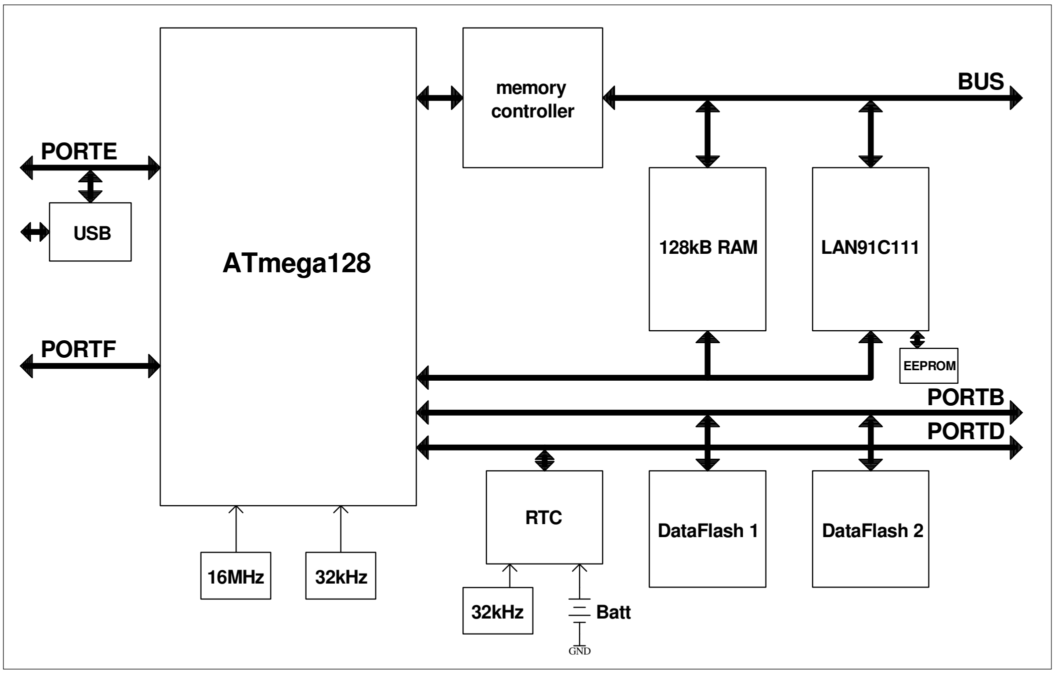


Figure 1 Block diagram of the MMnet104 minimodule.

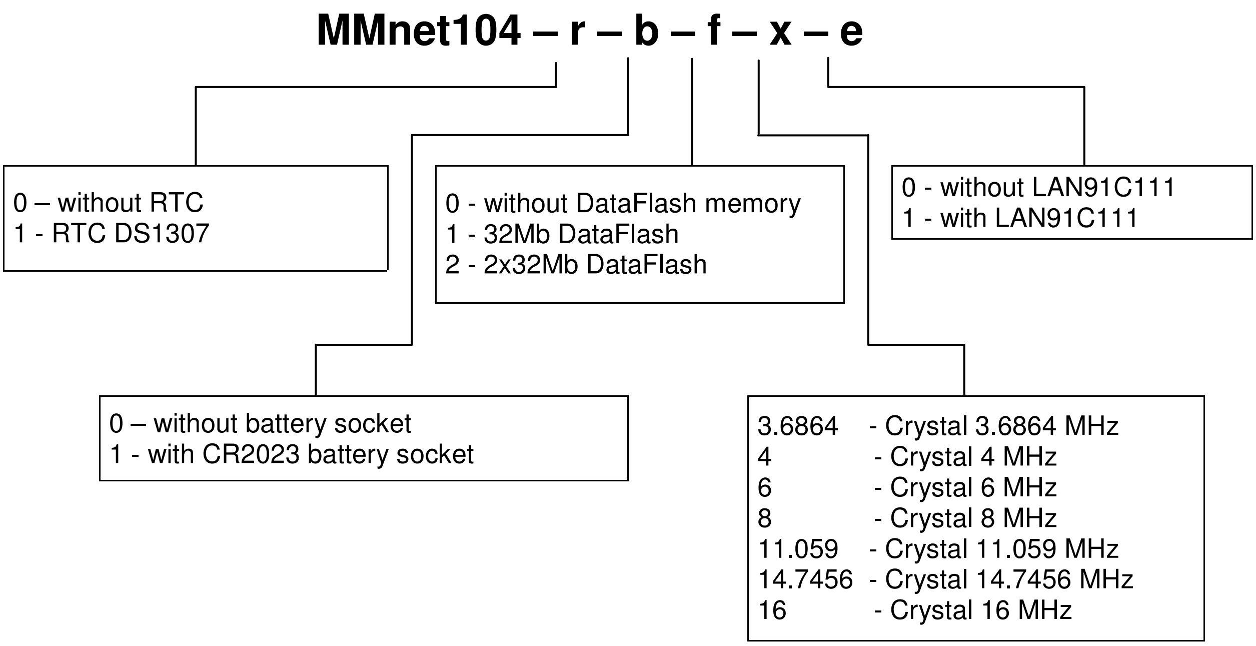
The minimodule is sold in three basic versions, denoted with letters from A to C, or in accordance with individual orders.

Module **MMnet104- A** contains:
- ATmega128 microcontroller
- Ethernet controller LAN91C111
- 128kB RAM

Module **MMnet104- B** contains:
- ATmega128 microcontroller
- Ethernet controller LAN91C111
- 128kB RAM
- One DataFlash 32Mb (4MB) memory
- Real Time Clock with socket for lithium battery

Module **MMnet104- C** contains:
- ATmega128 microcontroller
- Ethernet controller LAN91C111
- 128kB RAM
- Two DataFlash memories with 64Mb (8MB) of total capacity
- Real Time Clock with socket for lithium battery

Individual orders coding:



Module pin-out

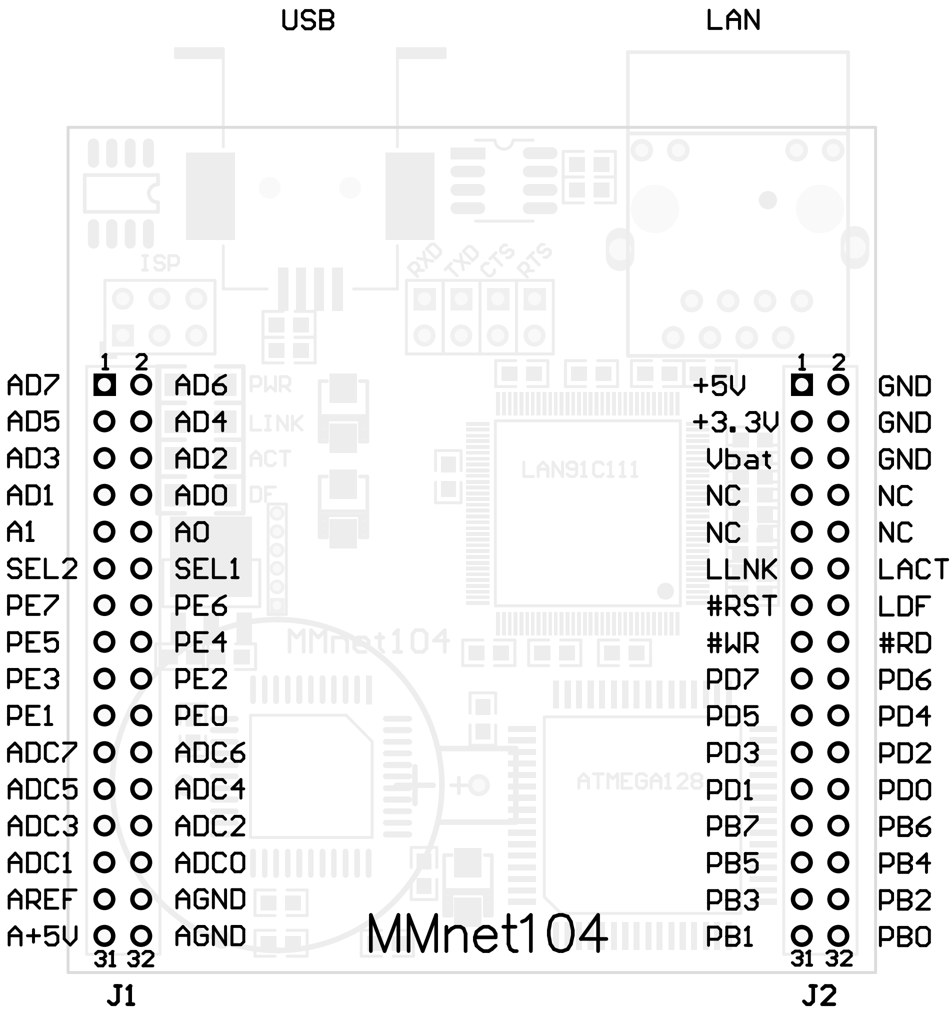


Figure 2 Module pin-out – top view.

J1

Function in MMnet104	Name	Pin	Pin	Name	Function in MMnet104
	AD7	**1**	**2**	AD6	
	AD5	**3**	**4**	AD4	
	AD3	**5**	**6**	AD2	
	AD1	**7**	**8**	AD0	
	A1	**9**	**10**	A0	
	SEL2	**11**	**12**	SEL1	
Interrupt from LAN91C111 (optionally)	PE7/ INT7	**13**	**14**	PE6/ INT6	
Interrupt from LAN91C111	PE5/ INT5	**15**	**16**	PE4/ INT4	
	PE3/ AC-	**17**	**18**	PE2/ AC+	
USB – TxD	PE1/ PDO/TxD	**19**	**20**	PE0/ PDI/RxD	USB – RxD
	PF7/ ADC7/TDI	**21**	**22**	PF6/ ADC6/TDO	
	PF5/ ADC5/TMS	**23**	**24**	PF4/ ADC4/TCK	
	PF3/ADC3	**25**	**26**	PF2/ ADC2	
	PF1/ ADC1	**27**	**28**	PF0/ ADC0	
	AREF	**29**	**30**	AGND	
	A+5V	**31**	**32**	AGND	

J2

Function in MMnet104	Name	Pin	Pin	Name	Function in MMnet104
	+5V	**1**	**2**	GND	
	+3.3V	**3**	**4**	GND	
	Vbat	**5**	**6**	GND	
	NC	**7**	**8**	NC	
	NC	**9**	**10**	NC	
	LEDLINK	**11**	**12**	LEDACT	
	#RESET	**13**	**14**	LEDDF	
	#WR	**15**	**16**	#RD	
	PD7/T2	**17**	**18**	PD6/ T1	
	PD5	**19**	**20**	PD4/ IC1	
	PD3/#INT3/TxD1	**21**	**22**	PD2/#INT2/RxD1	
RTC – SDA	PD1/#INT1/SDA	**23**	**24**	PD0/#INT0/SCL	RTC – SCL
	PB7/ OC2/PWM2	**25**	**26**	PB6/OC1B/PWM1B	DataFlash2 - #CS
DataFlash1 – #CS	PB5/ OC1A/PWM1A	**27**	**28**	PB4/OC0/PWM0	
DataFlash1/2 – MISO	PB3/ MISO	**29**	**30**	PB2/MOSI	DataFlash1/2 - MOSI
DataFlash1/2 – SCK	PB1/ SCK	**31**	**32**	PB0/#SS	

J1			
No.	**Function**	**Alt. function**	**Description**
1	AD7		Data bus. Allows connecting externals peripherals mapped in microcontroller address space. Peripheral addressing is done with use of SEL1, SEL2 and/or A0, A1, #WR, #RD outputs.
2	AD6		
3	AD5		
4	AD4		
5	AD3		
6	AD2		
7	AD1		
8	AD0		
9	A1		Lowest two bits of address bus. Allows addressing 4 input and 4 output registers. Note: outputs operate in 3.3V logic level standard.
10	A0		
11	SEL2		Read/write strobe or address decoder outputs. Note: outputs operate in 3.3V logic level standard.
12	SEL1		
13	PE7	INT7	PE7 – General purpose digital I/O Alternative functions: INT7 – External Interrupt source 7: The PE7 pin can serve as an external interrupt source. IC3 – Input Capture Pin3: The PE7 pin can act as an input capture pin for Timer/Counter3.
14	PE6	INT6	PE6 – general purpose digital I/O Alternative functions: INT6 – External Interrupt source 6: The PE6 pin can serve as an external interrupt source. T3 – Timer/Counter3 counter source.
15	PE5	INT5	PE5 – general purpose digital I/O Alternative functions: INT5 – External Interrupt source 5: The PE5 pin can serve as an External Interrupt source. OC3C – Output Compare Match C output: The PE5 pin can serve as an External output for the Timer/Counter3 Output Compare C. The pin has to be configured as an output (DDE5 set “one”) to serve this function. The OC3C pin is also the output pin for the PWM mode timer function.
16	PE4	INT4	PE4 – general purpose digital I/O Alternative functions: INT4 – External Interrupt source 4: The PE4 pin can serve as an External Interrupt source. OC3B – Output Compare Match B output: The PE4 pin can serve as an External output for the Timer/Counter3 Output Compare B. The pin has to be configured as an output (DDE4 set (one)) to serve this function. The OC3B pin is also the output pin for the PWM mode timer function.
17	PE3	AC-	PE3 – general purpose digital I/O Alternative functions: AC- – Analog Comparator Negative input. This pin is directly connected to the negative input of the Analog Comparator. OC3A, Output Compare Match A output: The PE3 pin can serve as an External output for the Timer/Counter3 Output Compare A. The pin has to be configured as an output (DDE3 set “one”) to serve this function. The OC3A pin is also the output pin for the PWM mode timer function.
18	PE2	AC+	PE2 – general purpose digital I/O Alternative functions: AC+ – Analog Comparator Positive input. This pin is directly connected to the positive input of the Analog Comparator. XCK0, USART0 External clock. The Data Direction Register (DDE2) controls whether the clock is output (DDE2 set) or input (DDE2 cleared). The XCK0 pin is active only when the USART0 operates in Synchronous mode.

19	PE1	PDO/TxD	PE1 – general purpose digital I/O Alternative functions: PDO – SPI Serial Programming Data Output. During Serial Program Downloading, this pin is used as data output line for the ATmega128. TXD0 – UART0 Transmit pin.
20	PE0	PDI/RxD	PE0 – general purpose digital I/O Alternative functions: PDI – SPI Serial Programming Data Input. During Serial Program Downloading, this pin is used as data input line for the ATmega128. RXD0 – USART0 Receive Pin. Receive Data (Data input pin for the USART0). When the USART0 receiver is enabled this pin is configured as an input regardless of the value of DDRE0. When the USART0 forces this pin to be an input, a logical one in PORTE0 will turn on the internal pull-up.
21	PF7	ADC7	PF7 – general purpose digital I/O Alternative functions: ADC7 – Analog to Digital Converter, Channel 7. TDI – JTAG Test Data In: Serial input data to be shifted in to the Instruction Register or Data Register (scan chains). When the JTAG interface is enabled, this pin can not be used as an I/O pin.
22	PF6	ADC6	PF6 – general purpose digital I/O Alternative functions: ADC6 – Analog to Digital Converter, Channel 6. TDO – JTAG Test Data Out: Serial output data from Instruction Register or Data Register. When the JTAG interface is enabled, this pin can not be used as an I/O pin. The TDO pin is tri-stated unless TAP states that shift out data are entered.
23	PF5	ADC5	PF5 – general purpose digital I/O Alternative functions: ADC5 – Analog to Digital Converter, Channel 5. TMS – JTAG Test Mode Select: This pin is used for navigating through the TAP-controller state machine. When the JTAG interface is enabled, this pin can not be used as an I/O pin.
24	PF4	ADC4	PF4 – general purpose digital I/O Alternative functions: ADC4 – Analog to Digital Converter, Channel 4. TCK – JTAG Test Clock: JTAG operation is synchronous to TCK. When the JTAG interface is enabled, this pin can not be used as an I/O pin.
25	PF3	ADC3	PF3 – general purpose digital I/O Alternative functions: ADC3 – Analog to Digital Converter, Channel 3.
26	PF2	ADC2	PF2 – general purpose digital I/O Alternative functions: ADC2 – Analog to Digital Converter, Channel 2.
27	PF1	ADC1	PF1 – general purpose digital I/O Alternative functions: ADC1 – Analog to Digital Converter, Channel 1.
28	PF0	ADC0	PF0 – general purpose digital I/O Alternative functions: ADC0 – Analog to Digital Converter, Channel 0.
29	AREF		Analog reference voltage for the A/D converter
30	AGND		Analog ground (internally connected with digital ground GND)
31	A+5V		+5V power supply for analog circuits. Connected internally with +5V through LP filter. External analog circuits can use this voltage.
32	AGND		Analog ground (internally connected with digital ground GND)

No.	Function	Alt. function	Description
1	+5V		Power supply input +5V
2	GND		Ground
3	+3.3V		Output of +3.3V voltage from internal regulator. Can be used to power external peripherals, which requires +3.3V.
4	GND		Ground
5	Vbat		Battery voltage sustaining the operation of the RTC clock. If a battery is mounted on the module, this lead-out can be used as a source of power for peripherals external to the module. If there is no battery on the module, the TC clock can be supplied from an external battery or another emergency power source.
6	GND		Ground
7	NC		Not connected.
8	NC		
9	NC		Not connected.
10	NC		
11	LEDLINK		The output of the LEDLINK diode driving signal (indicating connection to the Ethernet network). It can be used to connect an additional diode, e.g. led out externally to the device case.
12	LEDACT		The output of the LEDACT diode driving signal (indicating activity of the module in Ethernet network). It can be used to connect an additional diode, e.g. led out externally to the device case.
13	#RESET		Input/output of RESET signal
14	LEDDF		The output of the LEDDF diode driving signal (indicating activity of the DataFlash memory). It can be used to connect an additional diode, e.g. led out externally to the device case.
15	#WR		Write strobe.
16	#RD		Read strobe.
17	PD7	T2	PD7 – general purpose digital I/O Alternative functions: T2 – Timer/Counter2 counter source.
18	PD6	T1	PD6 – general purpose digital I/O Alternative functions: T1 – Timer/Counter1 counter source.
19	PD5		PD5 – general purpose digital I/O
20	PD4	IC1	PD4 – general purpose digital I/O Alternative functions: XCK1 – USART1 External clock. The Data Direction Register (DDD4) controls whether the clock is output (DDD4 set) or input (DDD4 cleared). The XCK1 pin is active only when the USART1 operates in Synchronous mode. IC1 – Input Capture Pin1: The PD4 pin can act as an input capture pin for Timer/Counter1.
21	PD3	#INT3/TxD1	PD3 – general purpose digital I/O Alternative functions: INT3 – External Interrupt source 3: The PD3 pin can serve as an external interrupt source to the MCU. TXD1 – Transmit Data (Data output pin for the USART1). When the USART1 Transmitter is enabled, this pin is configured as an output regardless of the value of DDD3.
22	PD2	#INT2/RxD1	PD2 – general purpose digital I/O Alternative functions: INT2 – External Interrupt source 2. The PD2 pin can serve as an External Interrupt source to the MCU. RXD1 – Receive Data (Data input pin for the USART1). When the USART1 receiver is enabled this pin is configured as an input regardless of the value of DDD2. When the USART forces this pin to be an input, the pull-up can still be controlled by the PORTD2 bit.

23	PD1	#INT1/SDA	PD1 – general purpose digital I/O Alternative functions: INT1 – External Interrupt source 1. The PD1 pin can serve as an external interrupt source to the MCU. SDA – Two-wire Serial Interface Data: When the TWEN bit in TWCR is set (one) to enable the Two-wire Serial Interface, pin PD1 is disconnected from the port and becomes the Serial Data I/O pin for the Two-wire Serial Interface. In this mode, there is a spike filter on the pin to suppress spikes shorter than 50 ns on the input signal, and the pin is driven by an open drain driver with slew-rate limitation.
24	PD0	#INT0/SCL	PD0 – general purpose digital I/O Alternative functions: INT0 – External Interrupt source 0. The PD0 pin can serve as an external interrupt source to the MCU. SCL – Two-wire Serial Interface Clock: When the TWEN bit in TWCR is set (one) to enable the Two-wire Serial Interface, pin PD0 is disconnected from the port and becomes the Serial Clock I/O pin for the Two-wire Serial Interface. In this mode, there is a spike filter on the pin to suppress spikes shorter than 50 ns on the input signal, and the pin is driven by an open drain driver with slew-rate limitation.
25	PB7	OC2/PWM2	PB7 – general purpose digital I/O Alternative functions: OC2 – Output Compare Match output: The PB7 pin can serve as an external output for the Timer/Counter2 Output Compare. The pin has to be configured as an output (DDB7 set “one”) to serve this function. The OC2 pin is also the output pin for the PWM mode timer function. OC1C – Output Compare Match C output: The PB7 pin can serve as an external output for the Timer/Counter1 Output Compare C. The pin has to be configured as an output (DDB7 set (one)) to serve this function. The OC1C pin is also the output pin for the PWM mode timer function.
26	PB6	OC1B/PWM1B	PB6 – general purpose digital I/O Alternative functions: OC1B – Output Compare Match B output: The PB6 pin can serve as an external output for the Timer/Counter1 Output Compare B. The pin has to be configured as an output (DDB6 set (one)) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.
27	PB5	OC1A/PWM1A	PB5 – general purpose digital I/O Alternative functions: OC1A – Output Compare Match A output: The PB5 pin can serve as an external output for the Timer/Counter1 Output Compare A. The pin has to be configured as an output (DDB5 set (one)) to serve this function. The OC1A pin is also the output pin for the PWM mode timer function.
28	PB4	OC0/PWM0	PB4 – general purpose digital I/O Alternative functions: OC0 – Output Compare Match output: The PB4 pin can serve as an eternal output for the Timer/Counter0 Output Compare. The pin has to be configured as an output (DDB4 set (one)) to serve this function. The OC0 pin is also the output pin for the PWM mode timer function.
29	PB3	MISO	PB3 – general purpose digital I/O Alternative functions: MISO – Master Data input, Slave Data output pin for SPI channel. When the SPI is enabled as a master, this pin is configured as an input regardless of the setting of DDB3. When the SPI is enabled as a slave, the data direction of this pin is controlled by DDB3. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB3 bit.

30	PB2	MOSI	PB2 – general purpose digital I/O Alternative functions: MOSI – SPI Master Data output, Slave Data input for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB2. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB2. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB2 bit.
31	PB1	SCK	PB1 – general purpose digital I/O Alternative functions: SCK – Master Clock output, Slave Clock input pin for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB1. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB1. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB1 bit.
32	PB0	#SS	PB0 – general purpose digital I/O Alternative functions: SS – Slave Port Select input. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB0. As a slave, the SPI is activated when this pin is driven low. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB0. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB0 bit. Table 31 and Table 32 relate the alternate functions of Port B to the overriding signals shown in Figure 33 on page 67. SPI MSTR INPUT and SPI SLAVE OUTPUT constitute the MISO signal, while MOSI is divided into SPI MSTR OUTPUT and SPI SLAVE INPUT.

Detailed description of PB, PD, PE ports can be found in ATmega128 microcontroller datasheets.

ATmega128 microcontroller

- High-performance RISC architecture, 121 instructions (most single clock cycle execution), 16 MIPS at 16MHz
- 128 KBytes of Flash memory
- 4K Bytes of SRAM memory
- 4K Bytes of EEPROM
- SPI Master/Slave interface
- Four internal timers/counters 8/16bit
- Two UART interfaces (up to 1Mbaud)
- Serial interface compatible with I2C
- In System Programming
- In Circuit Debugging through JTAG interface
- Real Time Clock with 32 kHz oscillator
- 8 channel 10-bti A/D converter
- 6 I/O ports
- 6 PWM outputs
- Extended temperature range, internal and external interrupt sources
- Internal watchdog timer
- More informations at Atmel's site

Ethernet controller LAN91C111

- One-chip Ethernet controller with
- IEEE 802.3 10/100Mb/s
- Internal 8kB SRAM memory for buffers
- Built-in data prefetch function to improve performance
- Full duplex/half duplex
- Support diagnostic LEDs

The module is adapted to operate with the network controller with the use of interrupts. The interrupt signal is applied to input INT5 (PE5) of the microcontroller.

The state of the Ethernet controller is signaled by two LED diodes: LNK – connection with the network, and ACT – active (transmission/reception).

The location of the controller in the address space is dependent upon the chosen operating mode of the memory controller.

Memory controller

The memory controller, built around the CPLD programmable device, controls the address space of the microcontroller, generates address strobe/selection signals to be exploited by the user and serves in banking of the RAM memory.

The memory controller can operate in three modes which differ in the placement of areas in the address space:

- Mode of conformity with the EVBedu.net and Ethernet 1 boards – only 32kB of RAM memory is available, situated in the range to 0x7FFF. The registers of the LAN91C111 circuit are under the addresses: 0x8000 – 0x9000. The rest of the RAM memory is not accessible.
- Memory banking mode. In order to exploit fully the whole memory, the address decoder facilitates the division of the memory into banks of 16kB each. In the range until 0x7FFF the basic unbanked memory is located. Under the addresses 0x8000 – 0xBFFF is the currently used memory bank. The choice of a bank is effected by writing its number to the bank register which is located under the address 0xFF00. In the location up to 0x7FFF (basic memory) always the last bank is visible. Such a solution is always favorable when programming is done in C language, as environment variables and buffers, often used in the program, can be held in the basic memory, while the space with the variable bank number can be used e.g. to collect measurement data, large tables or buffers, the access to which is not hampered by a change in bank number. The Ethernet controller is under the address 0xC000.
- Maximum linear memory mode – the Ethernet controller is at the end of the address space under the address 0xFF80. The linear memory reaches the address 0xFEFF. This mode permits the achievement of a large linearly addressed memory of the size of 65280B.

The memory controller allows also the generation of two signals: SEL1 and SEL2. These signals can be configured as write/read strobe lines or address choice with any polarization. The configuration is achieved by means of appropriate registers.

The address space of the microcontroller under the addresses 0xFF00 to 0xFFFF contains an area reserved for MMnet104. It has two registers: a configuration and bank select registers, an area for the peripherals controlled by the SEL outputs and an area for the Ethernet controller.

This is depicted in the picture below:

	…	
FF80 – FF9F	LAN91C111	Ethernet ctrl registers
	…	
FF08 – FF0B	MMnet104_SEL2	External I/O
FF04 – FF07	MMnet104_SEL1	External I/O
	…	
FF01	MMnet104_CONF	Configuration register
FF00	MMnet104_BANKSR	Bank select register

The MMnet104_BANKSR register contained under the address 0xFF00 is used for the choice of an active RAM memory bank. The contents of this register have a meaning only when mode 1 of the memory controller is chosen. The register has only four lowest bits, during readout the remaining bits (4 – 7) have the value „0" and the value written into them has no meaning.

MMnet104_BANKSR 0xFF00

-	-	-	-	BANKSR3	BANKSR2	BANKSR1	BANKSR0
7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Under the address 0xFF01 is the configuration register of the memory controller. Through this register the operating mode of the controller and the SEL output can be chosen. Configuration should be set after every system reset.

MMnet104_CONF 0xFF01

SEL2POL	SEL2CFG1	SEL2CFG0	SEL1POL	SEL1CFG1	SEL1CFG0	MODE1	MODE0
7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W

The meaning of individual bits in the MMnet104_CONF register is shown by the table below:

No.	Name	Description
7	SEL2POL	SEL2 output polarization. „0" – active low level
6 5	SEL2CFG1 SEL2CFG0	Operating mode of SEL2 output
4	SEL1POL	SEL1 output polarization. „0" – active low level
3 2	SEL1CFG1 SEL1CFG0	Operating mode of SEL1 output.
1 0	MODE1 MODE0	Operating mode of the address decoder.

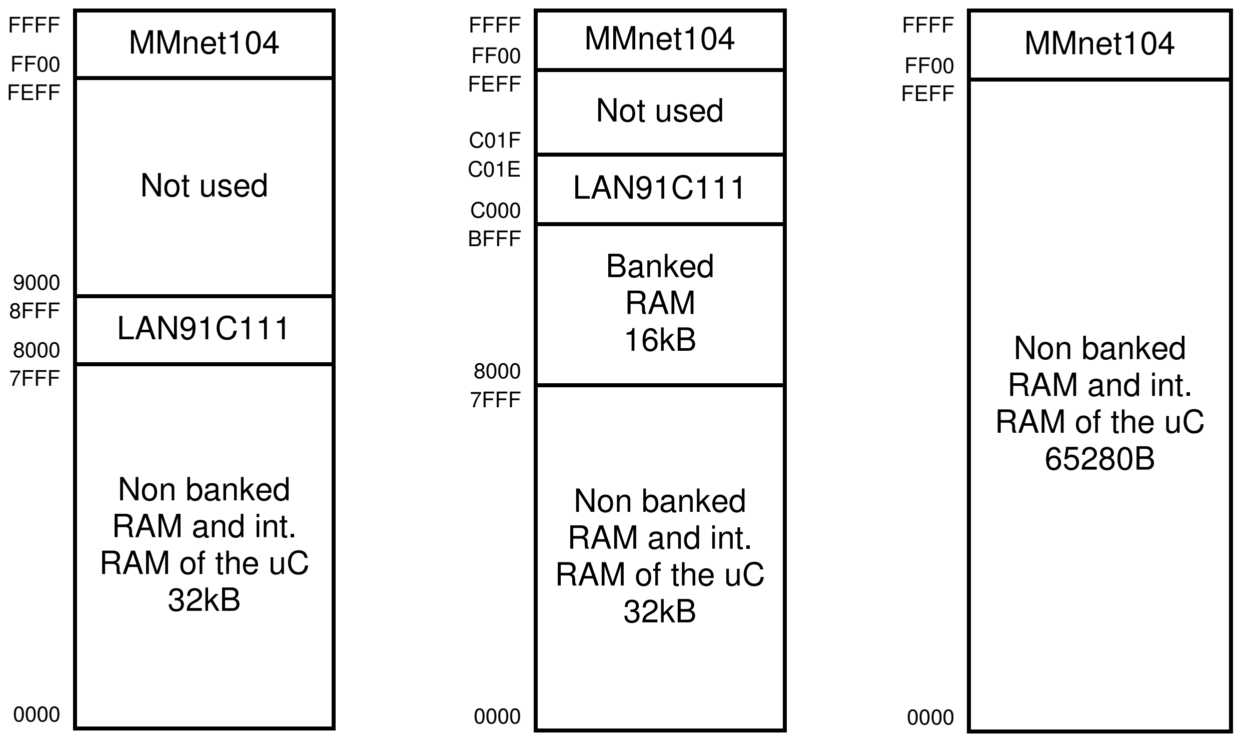
This register is assigned only for writing. An attempt of readout will return only random values.

Two lowest bits of the MMnet104_CONF register, assigned as MODE1 and MODE2, serve to set the operating mode of the address decoder:

Mode	MODE1..0	Description
0	00	**Conformity mode with earlier equipment and software versions.** Available is only 32kB of RAM memory located in the lower area of the address space, and the Ethernet controller under the addresses 0x8000-0x9000.
1	01	**Memory banking mode.** 32kB of non-banking memory is available; the remaining memory is accessible in banks of 16kB each. The Ethernet controller is under the address 0xC000.
2	10	**Mode of maximum linear memory.** In this mode the user has at his disposal 65280 memory bites without the need to serve banking. The LAN91C111 controller is under the address 0xFF80.

3	11	In this mode the external RAM memory and the Ethernet controller are not accessible. SEL outputs operate normally.

Memory maps for modes 1..3 are shown in the picture below:



Mode 0 **Mode 1** **Mode 2**

The remaining bits of the configuration register serve to set the operating mode of the SEL outputs and their polarization.

Mode	SEL1CFG1..0	Description
0	00	**Write strobe.** A pulse is generated at the moment of writing under the address 0xFF04 – 0xFF07. Polarization of the pulse is set by the SEL1POL bit.
1	01	**Read strobe.** A pulse is generated at the moment of reading under the address 0xFF04 – 0xFF07. Polarization of the pulse is set by the SEL1POL bit.
2	10	**Address decoder.** A pulse is generated at the moment of writing or reading from the address 0xFF04-0xFF07. Polarization of the pulse is set by the SEL1POL bit.
3	11	**Additional output.** Signal SEL1 assumes the value of the SEL1POL bit.

Mode	SEL2CFG1..0	Description
0	00	**Write strobe.** A pulse is generated at the moment of writing under the address 0xFF08 – 0xFF0B. Pulse polarization is set by the SEL2POL bit.
1	01	**Read strobe.** A pulse is generated at the moment of reading under the address 0xFF08 – 0xFF0B. Pulse polarization is set by the SEL2POL bit.
2	10	**Address decoder.** A pulse is generated at the moment of writing or reading under the address 0xFF08 – 0xFF0B. Pulse polarization is set by the SEL2POL bit.
3	11	If the module is fitted with a 256kB of RAM memory, output SEL2 is used as the highest bit of the address bus (in this case it must operate in mode 3) and cannot be used outside the module. If the module is fitted with a 128kB of RAM memory, output SEL2 in mode 3 can be used as additional output. It takes then the state of bit 3 in the MMnet104_BANKSR register.

The drawings below illustrate the operation of output SEL during writing or reading operation.

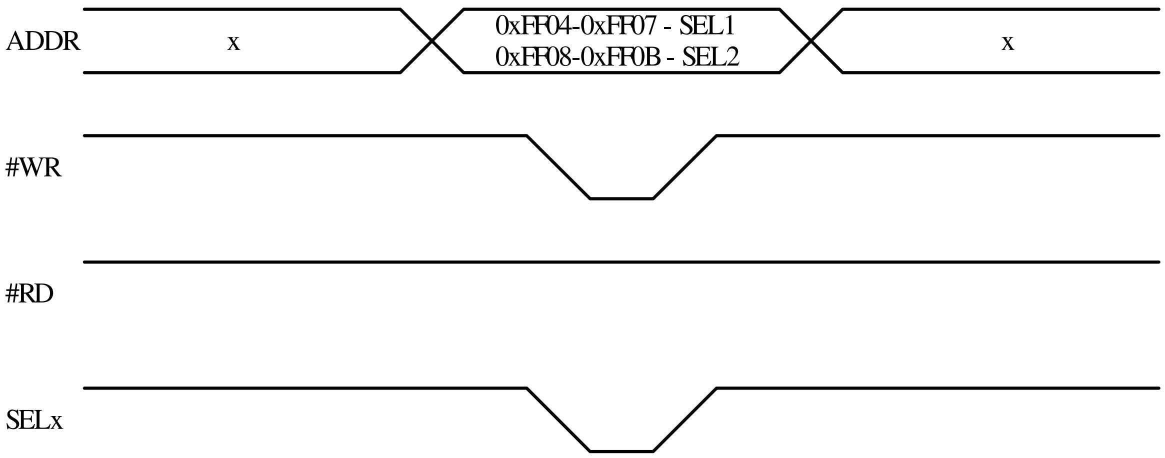


Figure 3 Operation of SEL output as write strobe (SELxCFG1..0=00) with active low level (SELxPOL = 0).

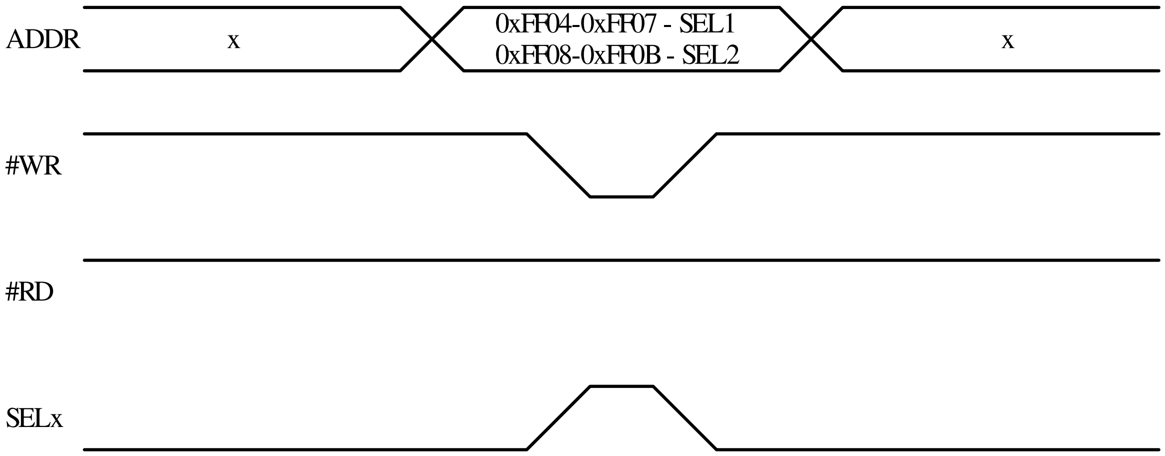


Figure 4 Operation of SEL output as write strobe (SELxCFG1..0=00) with active high level (SELxPOL = 1).

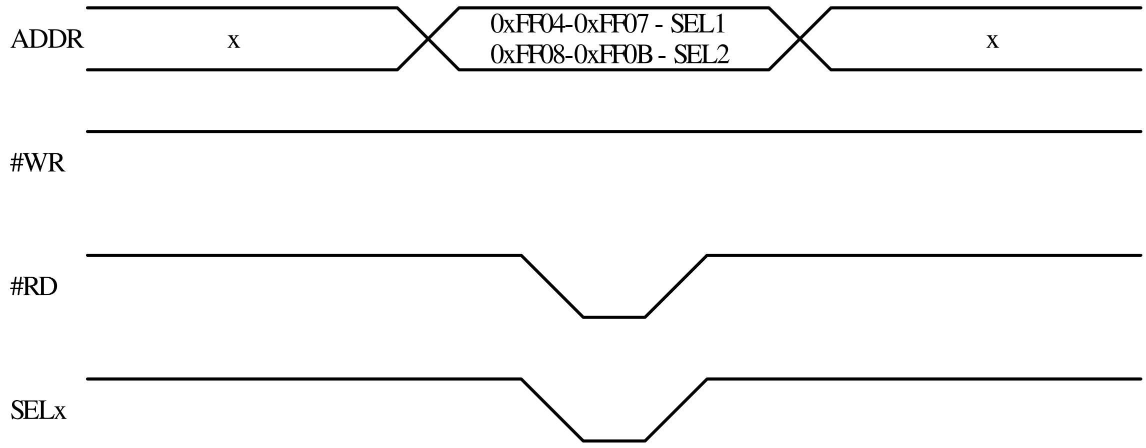


Figure 5 Operation of SEL output as read strobe (SELxCFG1..0=01) with active low level (SELxPOL = 0).

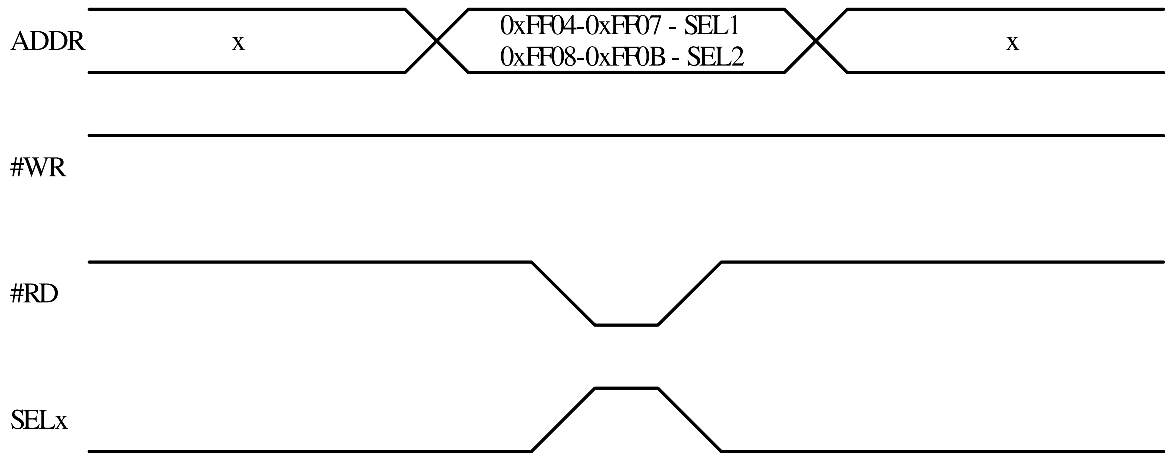


Figure 6 Operation of SEL output as read strobe (SELxCFG1..0=01) with active high level (SELxPOL = 1).

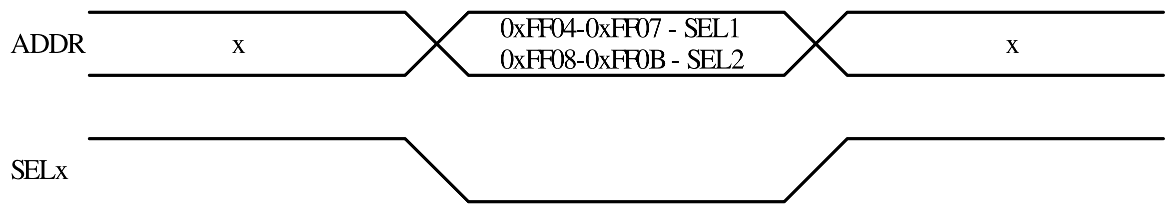


Figure 7 Operation of SEL output as address decoder (SELxCFG1..0=10) with active low level (SELxPOL = 0).

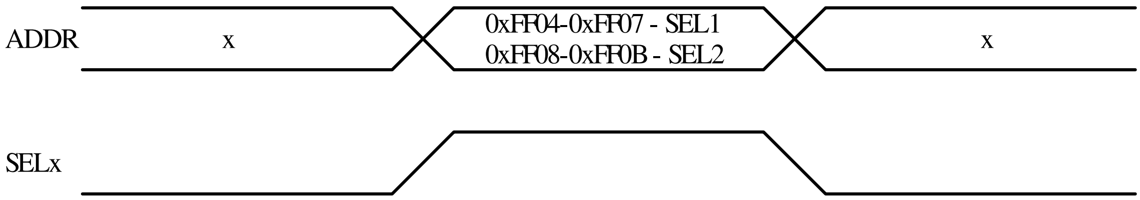


Figure 8 Operation of SEL output as address decoder (SELxCFG1..0=10) with active high level (SELxPOL = 1).

RAM memory

As a standard, the minimodule is equipped with a 128kB RAM memory. Because this is more than the ATmega128 microcontroller is able to address, it is necessary to bank the memory. This action is taken over by the memory controller.

Upon request, the microcontroller can be equipped with a 256kB RAM memory. The additional memory capacity is seen by the system as consecutive banks to choose from. In such a case the operating mode of the SEL2 signal must be set to 3 and the SEL2 output cannot be used outside the module.

DataFlash memory

The minimodule can be equipped with one or two serial DataFlash memories AT45DB321B with 32 Mb or 64 Mb (total capacity), this gives 4 or 8 MB of memory for storing files with WWW pages or collecting measurement files. The memories are connected to a fast SPI bus with 8 MB/s transmission speed.

Memory chips are activated after applying a low logic level to #CS inputs. The #CS pin of memory No.1 is connected to port PB5 of the microcontroller, and that of memory No.2 to port PB6. The SPI bus occupies three terminals of the microprocessor: PB1, PB2, PB3. It should be kept in mind that if DataFlash memories are installed, the just outlined port terminals cannot be used externally to the module. Of course the SPI bus can be used for communication with external peripherals, under the condition that they will have circuit selection inputs (CS). The diagram below shows the connection of DataFlash memories inside the module.

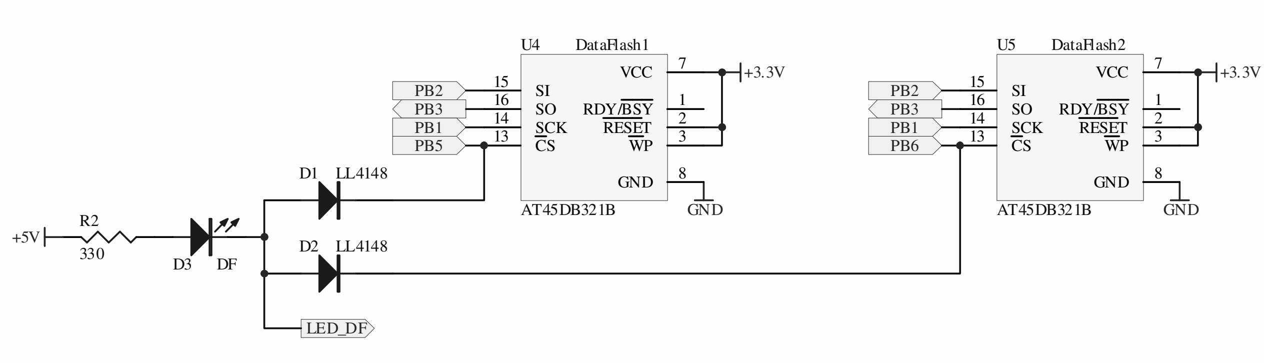


Figure 9 Connection of DataFlash memory inside the module.

A detailed description of DataFlash circuits is on the Atmel Company page: www.atmel.com .

Real-time clock

An additional device of the minimodule is the RTC clock operating with the DS1307 circuit connected to the I2C bus. Along with the RTC circuit, there is a socket for lithium batteries mounted on the module, providing a guarantee of many years of uninterrupted operation of the clock. The battery voltage is fed outside the module, allowing supplying power to other elements from one battery or taking electric supply from the outside. The I2C bus occupies two minimodule port terminals: PD0 and PD1. If the RTC clock is mounted, these terminals can be used only as an I2C bus communicating with other peripherals, they cannot, however, act as I/O ports.

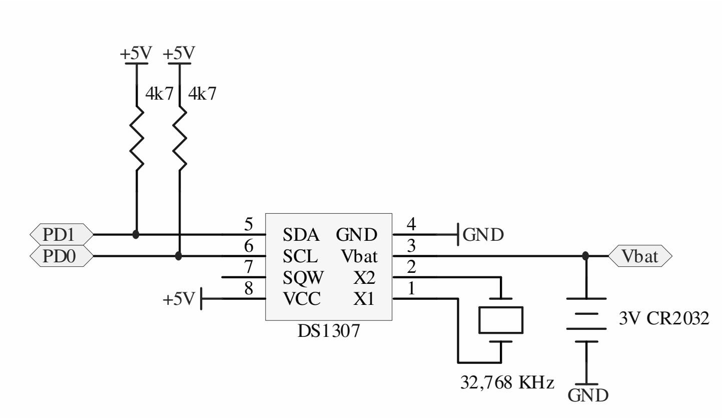


Figure 10 Connection of the RTC circuit inside the module.

A detailed description of the DS1307 circuit is given on the Maxim Company page: www.maxim-ic.com .

Supply of power

The module requires a regulated + 5 V supply voltage. The + 3.3 V voltage, indispensable for the operation of some circuits, is produced inside the module. It is also led out externally to be used by other system elements.

RESET circuit

The MMnet104 has a built-in voltage monitoring circuit constructed around the DS1811 integrated circuit. The circuit generates a RESET signal in case when the supply voltage value is lower than 4.6 V. This takes place when the supply voltage is switched on or off, when the VCC voltage changes its value from 0 to 5 V.

The guard circuit detects also momentary VCC voltage drops. A short duration drop of VCC below 4.6 V causes the generation of a resetting signal of 100 ms duration. This signal is applied directly to the resetting input of the microcontroller and through a simple inverter to the LAN91C111 circuit. The RESET signal is led out to a module connector and it can be used as the zeroing output resetting external circuits and as the input for resetting the module, e.g. by means of the RESET button. In such a case the RESET button can short the RESET line directly to ground. An implementation of the reset circuit is presented in the diagram below.

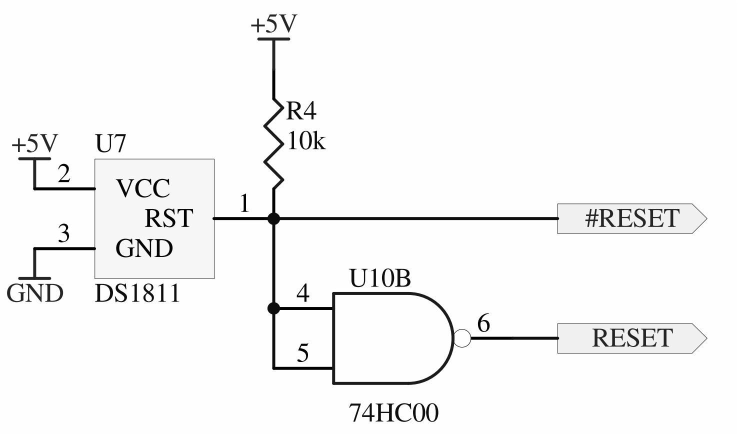


Figure 11 Implementation of the reset circuit in the module.

LED diodes

The minimodule is equipped with four LED diodes which signal the following:

- supply of power
- operation of the Ethernet controller:
    - connection to the network
    - activity (transmission/reception)
- operation of the DataFlash memory (analogously as the HDD diode in PCs).

Diode signals are led out outside the module which enables doubling the signaling e.g. externally to the device case. An example of a realization of such a solution is shown in the drawing:

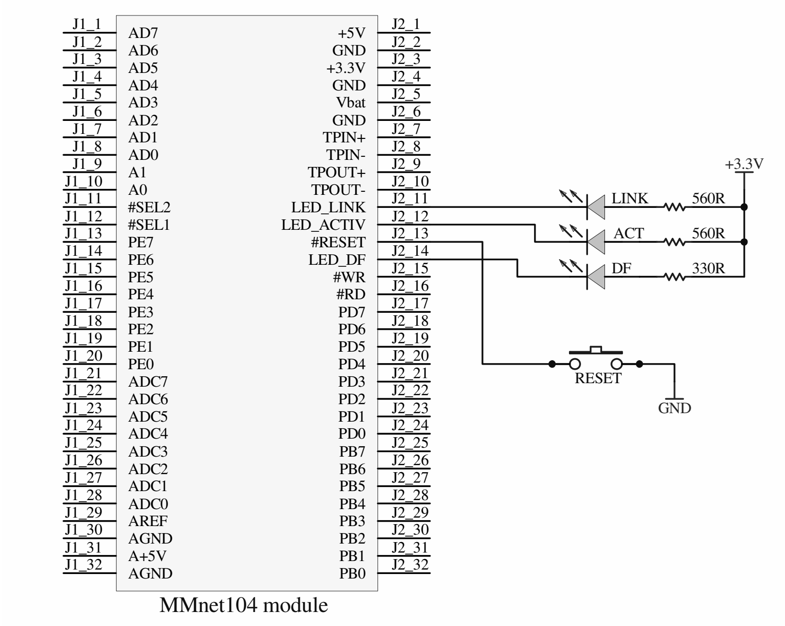


Figure 12 Connection of external signaling diodes and the RESET button.

Notice: the method of operation of diodes signaling the work of the Ethernet controller depends on the settings of its internal registers. The default configuration assures operation in accordance with the description on the module (LINK and ACT). If the RTC8019AS should use an external EEPROM memory storing configurations, or emulation of such memory, it should be kept in mind to set properly the bits configuring the operation of diodes (bits LEDS0 and LEDS1 in the CONFIG3 register should be set).

3 Connection of the module with the external world

Connection to the Ethernet network

The minimodule is equipped with RJ45 connector with integrated magnetics and LED diodes.

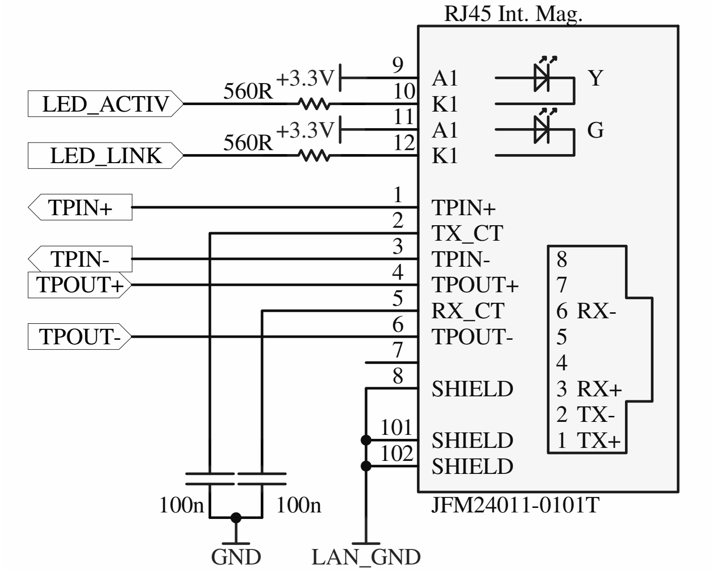


Figure 13 Connection of the Ethernet connector inside the module.

USB interface

MMnet104 has onboard USB port (device), which can be connected to USART0 (TXD0 and RXD0) through JP2 and JP4 jumpers. In addition, with use of JP3 and JP5 jumpers, flow control signals CTS and RTS can be connected to PE3 and PE2 ports. Implementation is based on FT232 IC, which appears to the microcontroller as standard RS-232 device.

Implementation of the RS-232 port is shown below:

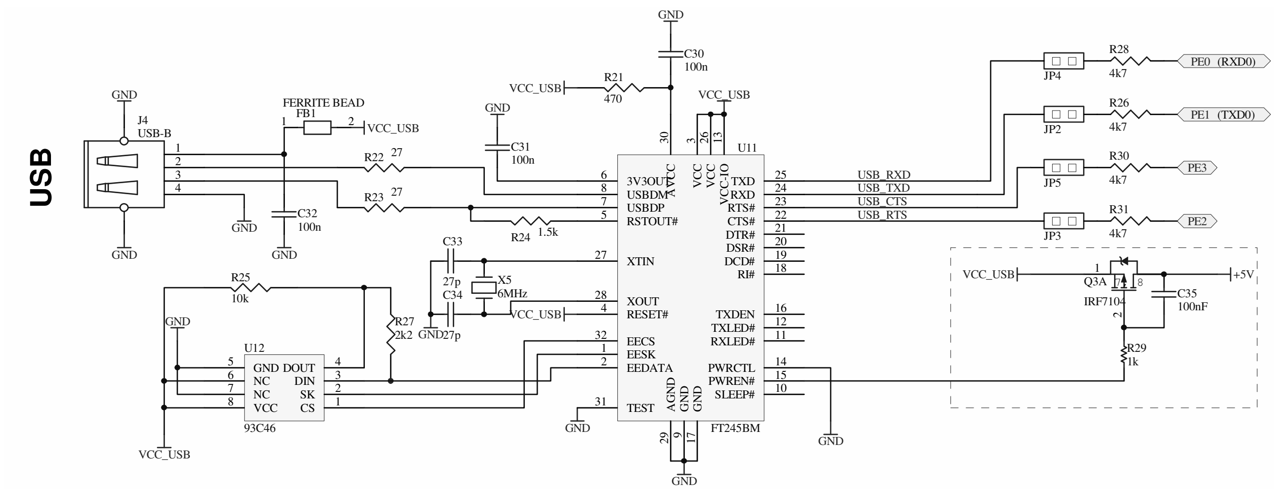
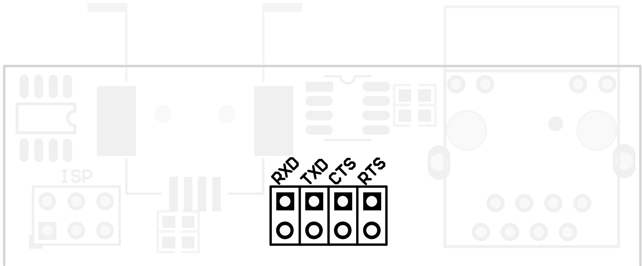
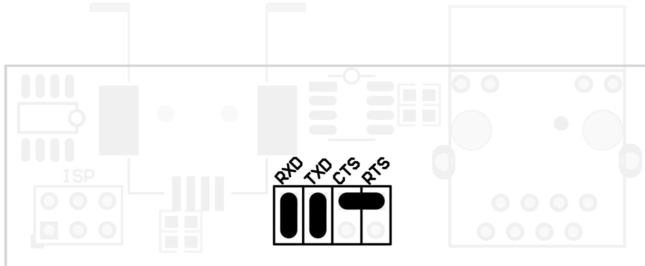


Figure 14 Implementatin of the USB port in MMnet104.



Placement of the USB configuration jumpers.



Typical jumpers configuration: TXD and RXD lines connected to microcontroller, CTS and RTS lines are not used and bypassed with the jumper.

RS-232 interface

RS-232 is the simplest communication interface, allowing connection of the module with PC or other device. To make that connection microcontroller's Txd and Rxd lines should be connected to level converter based on MAX232 or similar IC.

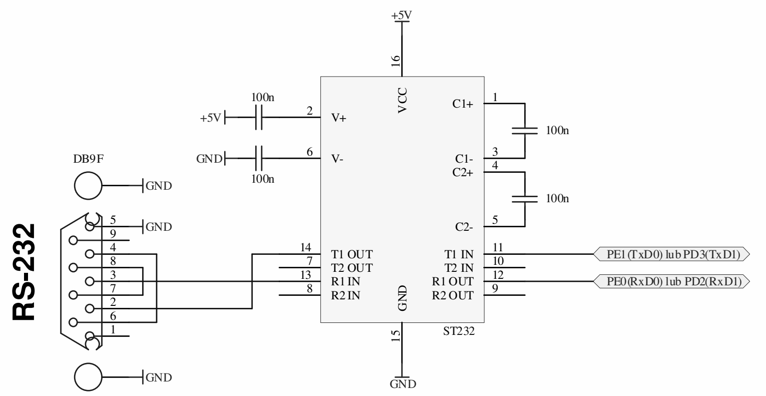


Figure 145 Connection of the RS-232 port to the MMnet104.

RS-485 interface

The RS-485 interface facilitates long-distance transmission in a difficult environment. An implementation of this interface is as simple as that of RS-232 and requires only a line driver, e.g. MAX485. The feature discerning this interface from RS-232 is the necessity to control the direction of action of the driver (transmission/reception). This control is effected through the program, using any I/O pin of the microcontroller. The 560R resistors visible in the diagram polarize initially the inputs, increasing the immunity to interference. The 120R resistor connected by means of a shorting strap is used to match the interface to the line impedance.

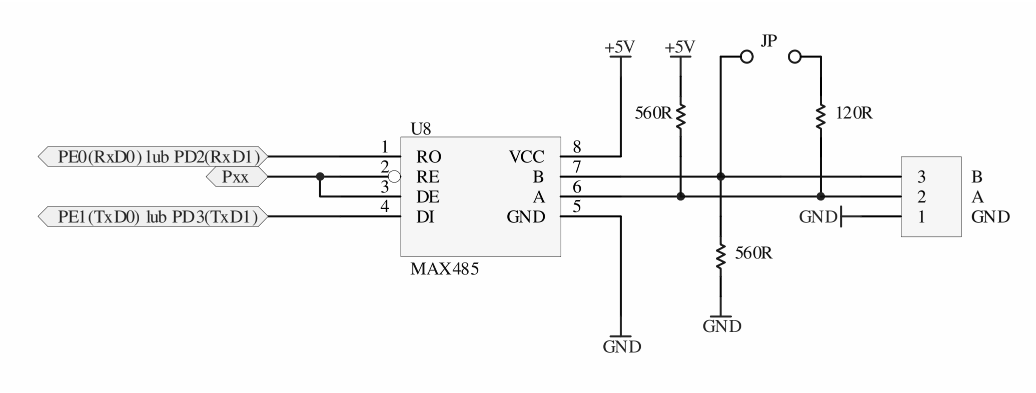
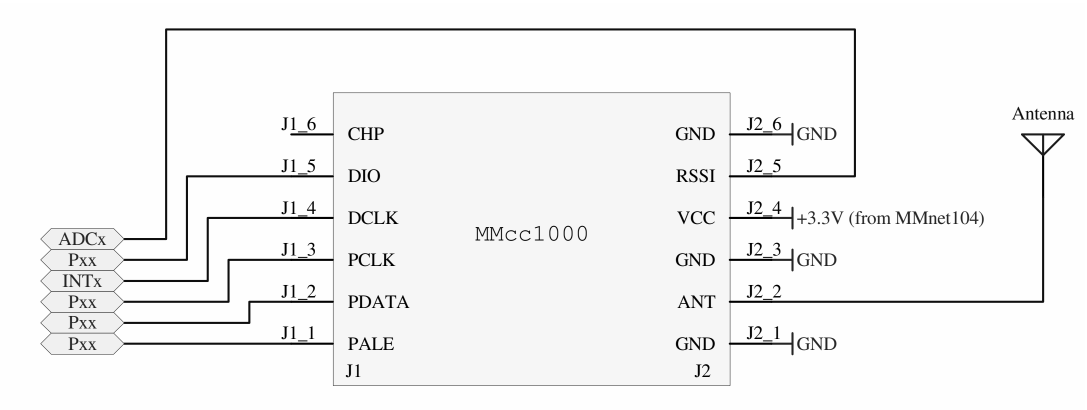


Figure 156 Connection of the RS-485 port to the MMnet104.

Radio link

Fitting the system with the possibility of communicating via a wireless path provides a possibility of easy control and collection of measurement data from system elements dispersed in the object, without the need to install any cabling. Thanks to the existence of integrated transceivers the construction of such links is relatively simple. The figure presents a way of connecting an MMnet104 module with a radio minimodule MMcc1000. To execute such a connection, five I/O microcontroller lines are needed, including one breakpoint input. An optional connection of the RSSI output with the input of the A/D converter permits the measurement of the strength of the received signal.



Additional information on the MMcc1000 module can be found on the page:
http://www.propox.com/products/t_92.html?lang=en

LCD display

The LCD display can be connected to the minimodule in several ways. The simplest of them is to use 7 I/O lines of the microcontroller and generating the necessary pulses by the program. Such a solution is shown in the figure below.

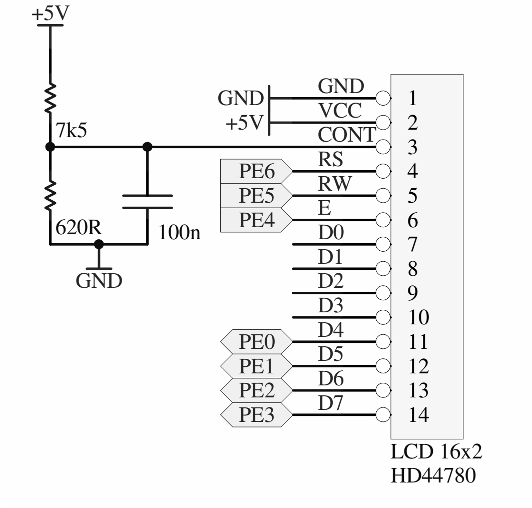


Figure 16 Connection of the LCD display to microcontroller ports.

Another way is to use the system bus led out from the module and the write strobe output. The method of connecting them is shown below:

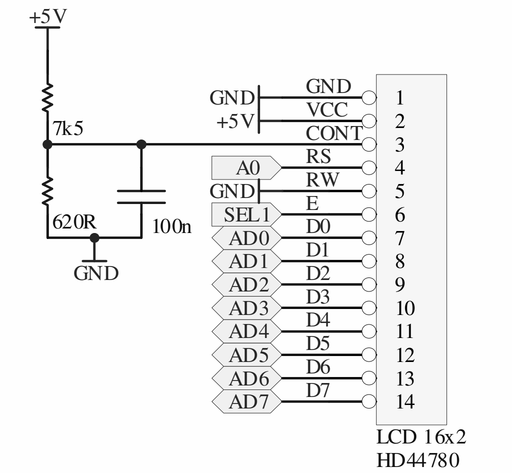


Figure 17 Connection of the LCD display to the microcontroller bus.

Such a connection method permits only the execution of a write operation into the display, which is sufficient. The SEL1 output should be configured as a write strobe. The display is seen in the address space as two registers: a command register under the address 0xFF04 and a data register under the address 0xFF05.

External peripherals on the system bus

External peripherals can be connected in a simple way to the module, thanks to the fact that the data bus, two bits of the address bus and universal SELx outputs were put out of the module. In the simplest case the SEL outputs will be used directly as the write/read strobe which will allow to locate two registers in the address space, without using additional address decoders. Such a case is depicted in the figure below.

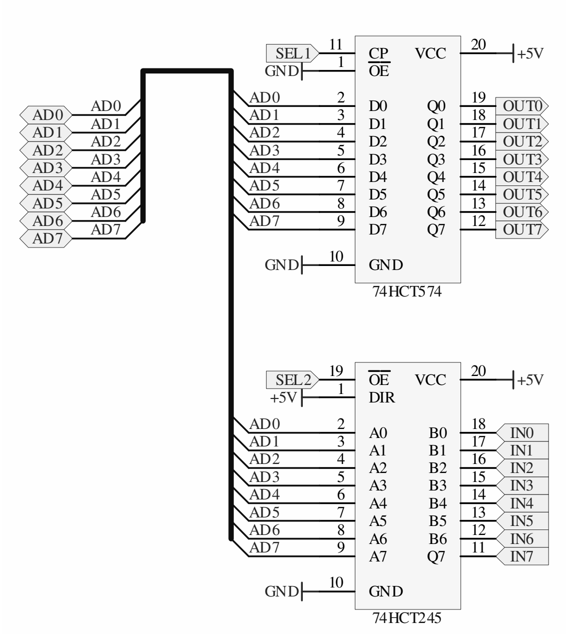


Figure 18 An example of using the SEL output and a write/read strobe.

The configuration and write/read methods of registers such connected looks like this:

```
MMnet104_CONF = 0b00100001;   // SEL2 - read strobe, active low,
                              // SEL1 - write strobe, active high,
                              // memory decoder mode 1
MMnet104_SEL1 = output_value; // write to output register
input_value = MMnet104_SEL2;  // read from input register
```

If a greater number of external I/O circuits are required, the SEL terminals can be used as address selection outputs. After connecting additional address decoders, e.g. 74HCT138, the number of registers possible to be addressed is increased to 4 output and 4 input registers. The configuration and write/read of registers may look like this:

```
MMnet104_CONF = 0b00100001;   // SEL2 - address decoder, active low,
                              // SEL1 - address decoder, active low,
                              // memory decoder mode 1
MMnet104_SEL1_0 = output_value_0;     // write to output register 0
MMnet104_SEL1_1 = output_value_1;     // write to output register 1
MMnet104_SEL1_2 = output_value_2;     // write to output register 2
MMnet104_SEL1_3 = output_value_3;     // write to output register 3


input_value_0 = MMnet104_SEL2_0;      // read from input register 0
input_value_1 = MMnet104_SEL2_1;      // read from input register 1
input_value_2 = MMnet104_SEL2_2;      // read from input register 2
input_value_3 = MMnet104_SEL2_3;      // read from input register 3
```

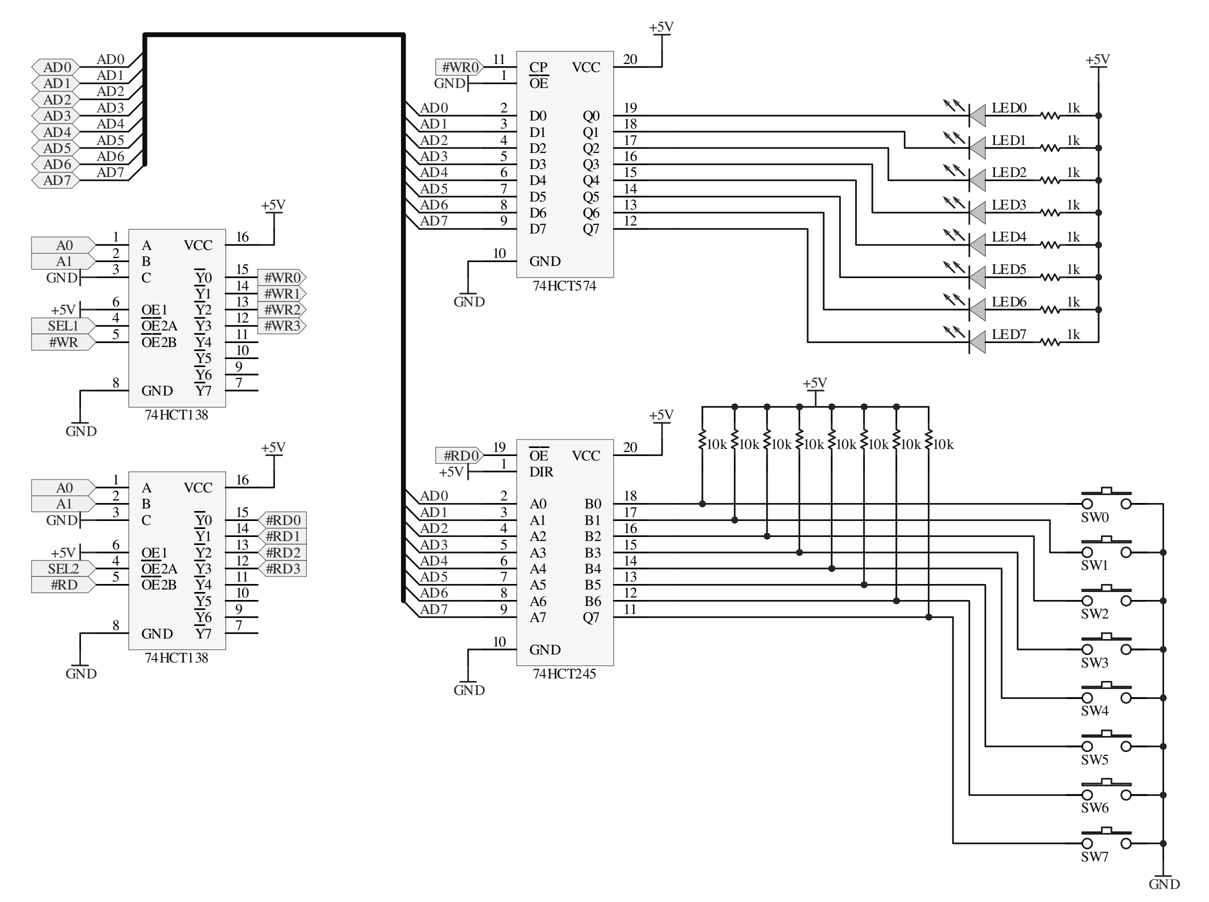


Figure 19 An example of using the SEL output as an address selection output.

4 Programming the module

The ATmega128 microcontroller has 128kB of Flash memory programmable in the system for the program code and 4kB of EEPROM memory for user's data. Programming of these memories can be effected in two ways: by means of an ISP interface or through JTAG. Both interfaces have a standard of used connectors and a standard of arranging signals in the connector.

ISP connector

The programmer in ISP standard communicates with the microcontroller through a three-wire SPI interface (plus the RESET signal and power supply). The interface uses the I/O terminals of the microcontroller (PE0, PE1 and PB1) which, after the programming, can fulfill ordinary functions. When connecting peripherals to these terminals it should be remembered that the programmer should have the possibility to force appropriate logic levels on them. The figures below present the method of connecting the ISP connector to the module. Figure 23 shows the use of an analog multiplexer 4053 to separate the programmer from the peripherals connected to microcontroller ports.

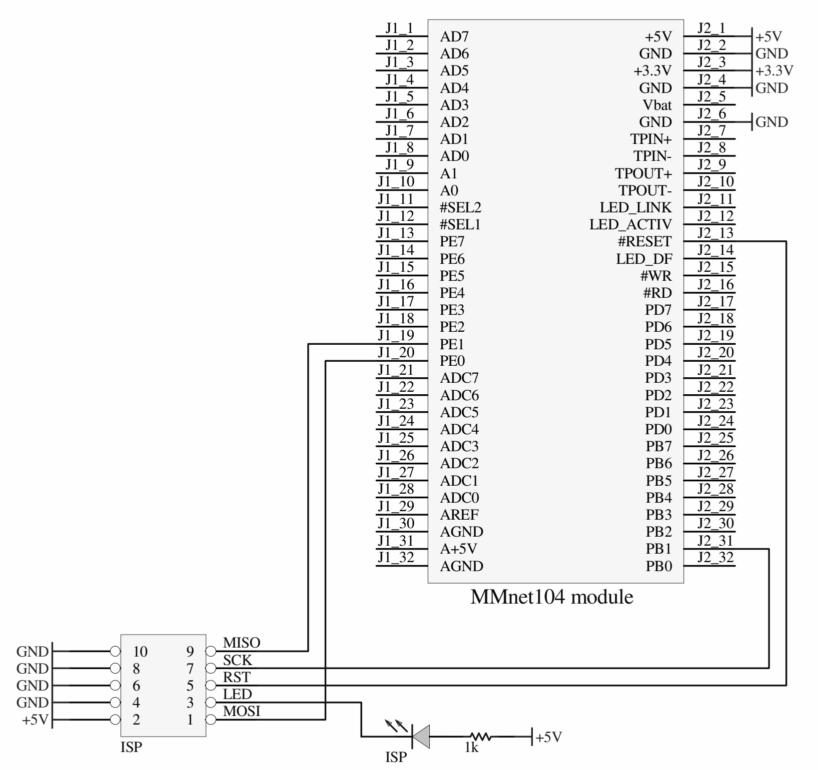


Figure 20 Connecting the MMnet104 module with an ISP connector.

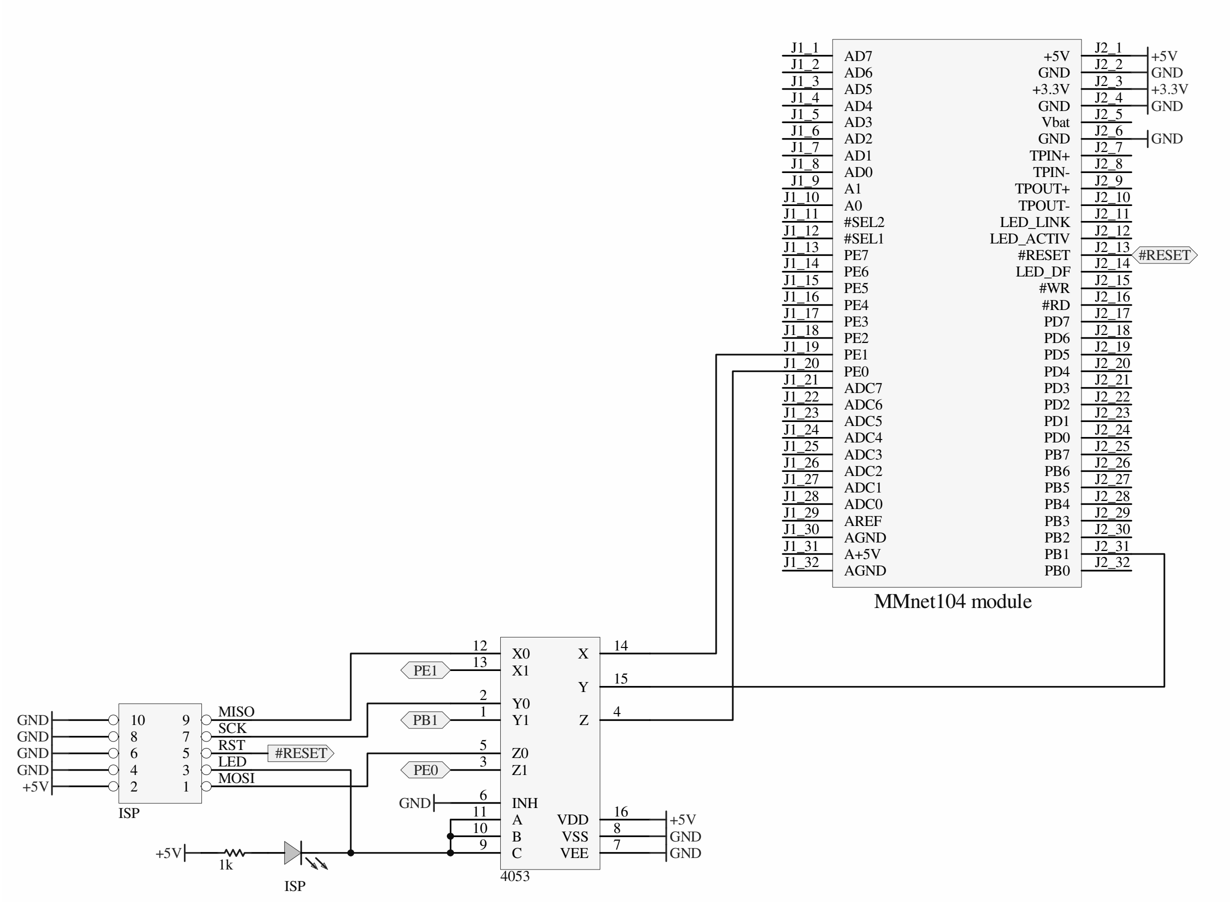


Figure 21 Connection of the MMnet104 module with an ISP connector using a multiplexer.

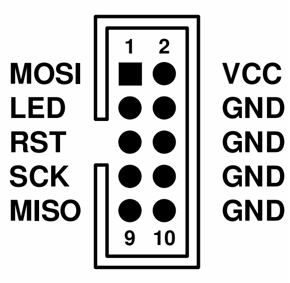
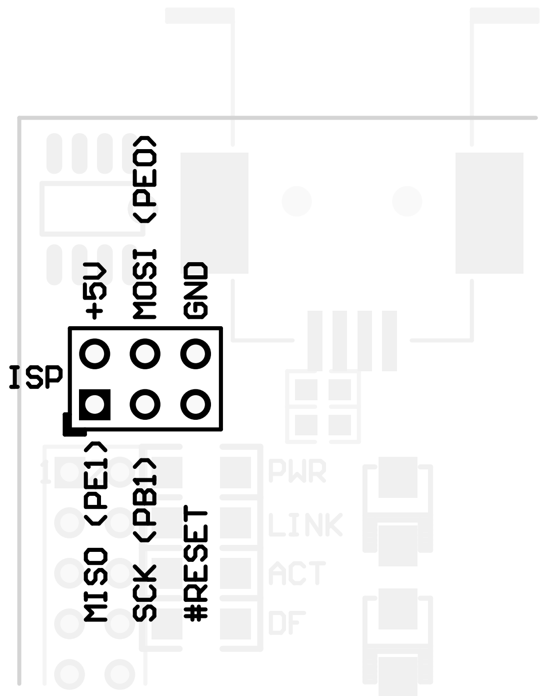


Figure 22 ISP connector.

PIN	DESCRIPTION
MOSI	Commands and data from programmer to target
LED	Multiplexer and LED diode driving signal
RST	RESET signal
SCK	Serial Clock, Controlled by programmer
MISO	Data from target AVR to programmer
VCC	Supply voltage to the programmer
GND	Ground

MMnet104 has also onboard ISP connector compatible with 6-pin Atmel standard. Pinout of this connector is shown on the drawing. Signals are directly connected to microcontroller’s port, without use of multiplexer.



Caution: The SPI interface used for programming the processor is not the same interface which is available to the user for communication with peripherals and it uses other outputs.

Programmers which can be used to program the MMnet104 can be found on the following pages:
- ISPCable I: http://www.propox.com/products/t_77.html?lang=en
- ISPCable II: http://www.propox.com/products/t_78.html?lang=en

JTAG connector

JTAG is a four-lead interface permitting the takeover of control over the processor’s core and its internal peripherals. The possibilities offered by this interface are, among others: step operation, full-speed operation, equipment and program pitfalls, inspection and modification of contents of registers and data memories. Apart from this, functions are available offered by ISP programmers: programming and readout of Flash, EEPROM, fuse memories and lock bites. The method of connecting the JTAG connector to the minimodule is shown in the drawing:

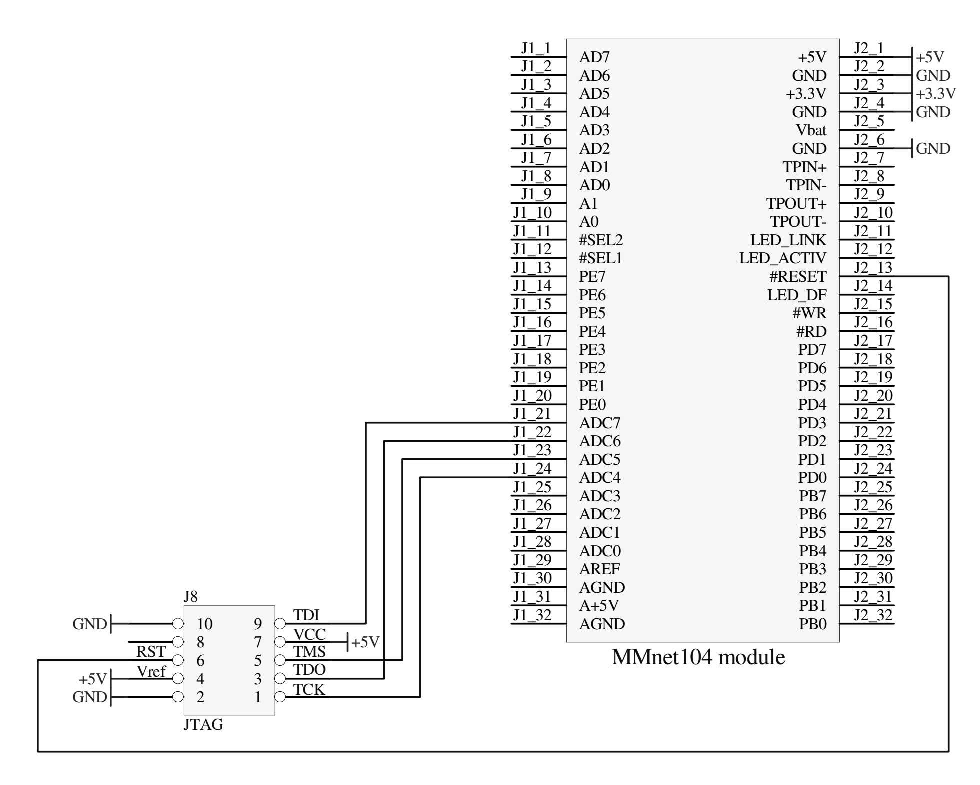


Figure 23 Connection of the MMnet104 module with the JTAG connector.

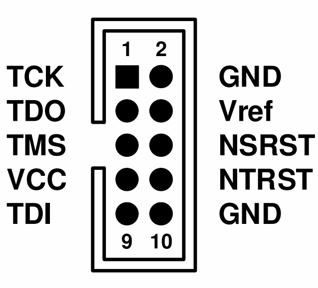


Figure 24 JTAG connector.

PIN DESCRIPTION

TCK	Test Clock, clock signal from emulator to target
TDO	Test Data Output, data signal from target to emul.
TMS	Test Mode Select, mode select signal from
VCC	Supply voltage to the emulator
TDI	Test Data Input, data signal from emul. to target
Vref	Target voltage sense
RST	RESET signal
GND	Ground

If the JTAG interface is connected into the fuse bits of the microcontroller, then terminals PF4...PF7 (ADC4...ADC7) can serve only as an interface and cannot operate as I/O terminals or analogue inputs.

The programmer/emulator JTAG can be found on the page:
- JTAGCable I : http://www.propox.com/products/t_99.html?lang=en

5 An application example

The diagram below shows the MMnet104 module in a simple application, controlling relays through the Ethernet network (e.g. surfing the WWW). The diagram does not include the supply of power.

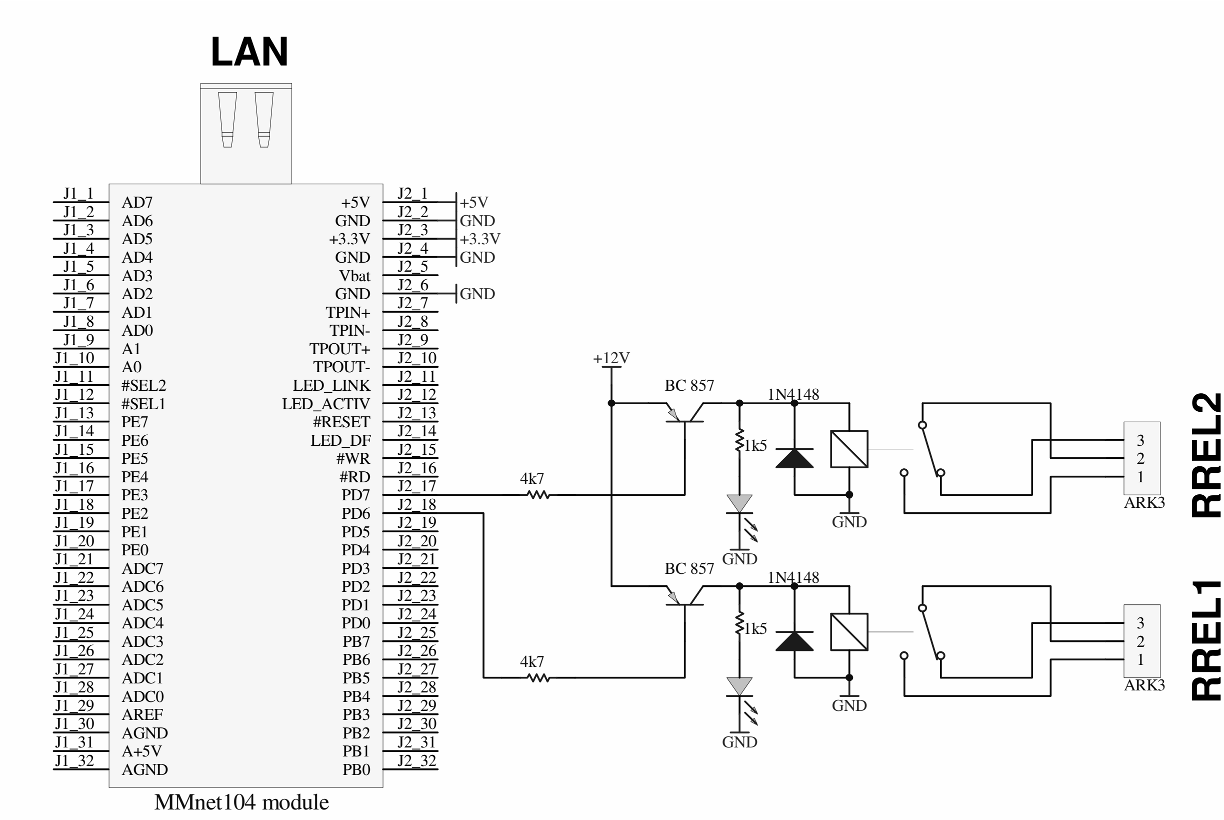


Figure 25 MMnet104 in a simple application controlling relays through the Ethernet network.

6 Evaluation Board

In order to facilitate the design of equipment using the minimodule, an evaluation board has been prepared (EVBnet03). It includes the following basic elements:

- Power supply
- USB port (with use of MMusb232 minimodule)
- ISP connector
- JTAG connector
- 2x16 chars LCD display
- 8 LED diodes
- 4 push-buttons
- 2 potentiometers
- Prototype design area



7 Specifications

Microcontroller	ATmega128 16MHz
Ethernet controller	LAN91C111 IEEE 802.3 10/100Mb/s
Program memory	128kB
Data memory	128kB or 256kB
EEPROM memory	8kB
DataFlash memory	up to 8MB
No. of digital I/O	up to 32
No. of analog inputs	up to 8
Power	5V 5%
Dimensions	56x59mm
Weight	about 100g
Operating temperature range	0 – 70ºC
Humidity	5 – 95%
Connectors	double 2x32 headers

8 Technical assistance

In order to obtain technical assistance please contact support@propox.com . In the request please include the following information:

- number of the module version (e.g. REV 2)
- setting of resistors
- a detailed description of the problem

9 Guarantee

The MMnet104 minimodule is covered by a six-month guarantee. All faults and defects not caused by the user will be removed at the Producer's cost. Transportation costs are borne by the buyer.

The Producer takes no responsibility for any damage and defects caused in the course of using the MMnet-02 module.

10 Assembly drawings

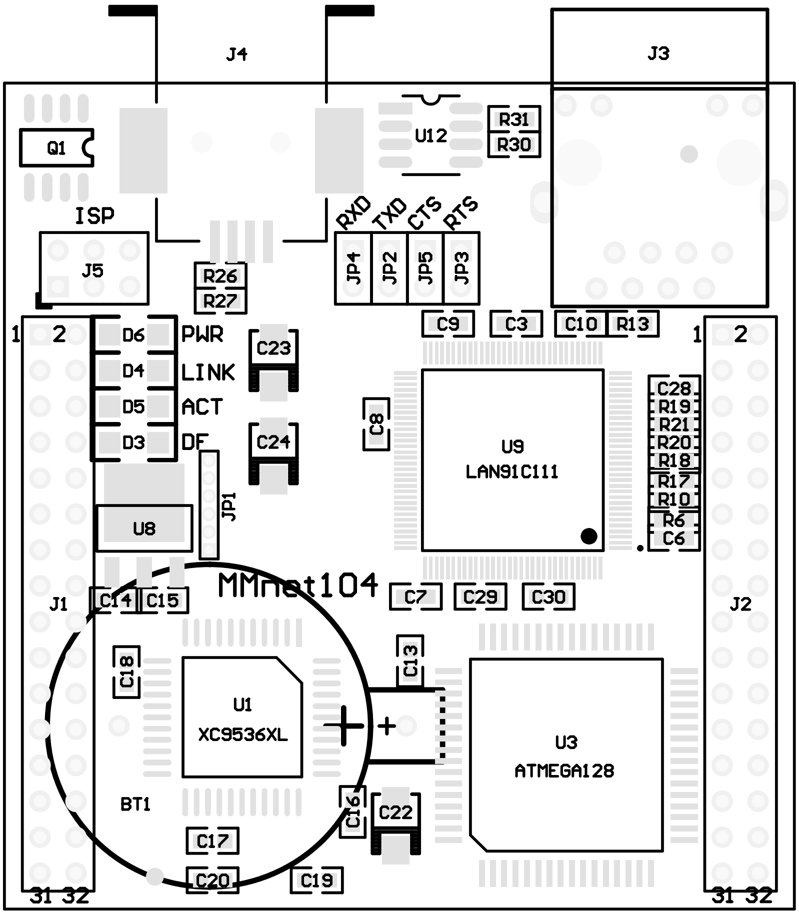


Figure 26 Assembly drawing – top layer.

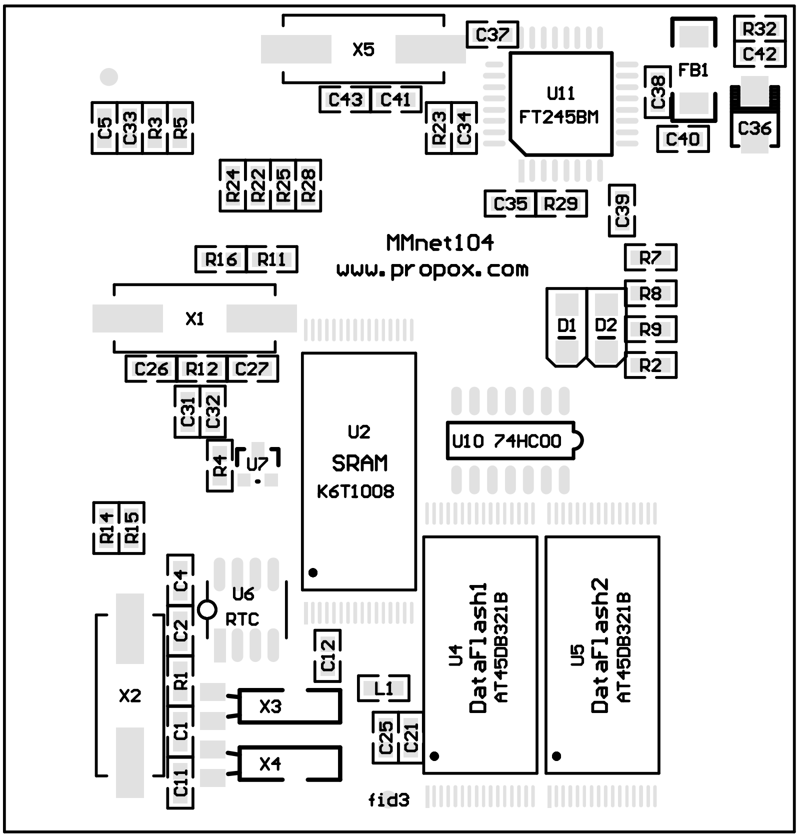


Figure 27 Assembly drawing – bottom layer.

11 Dimensions

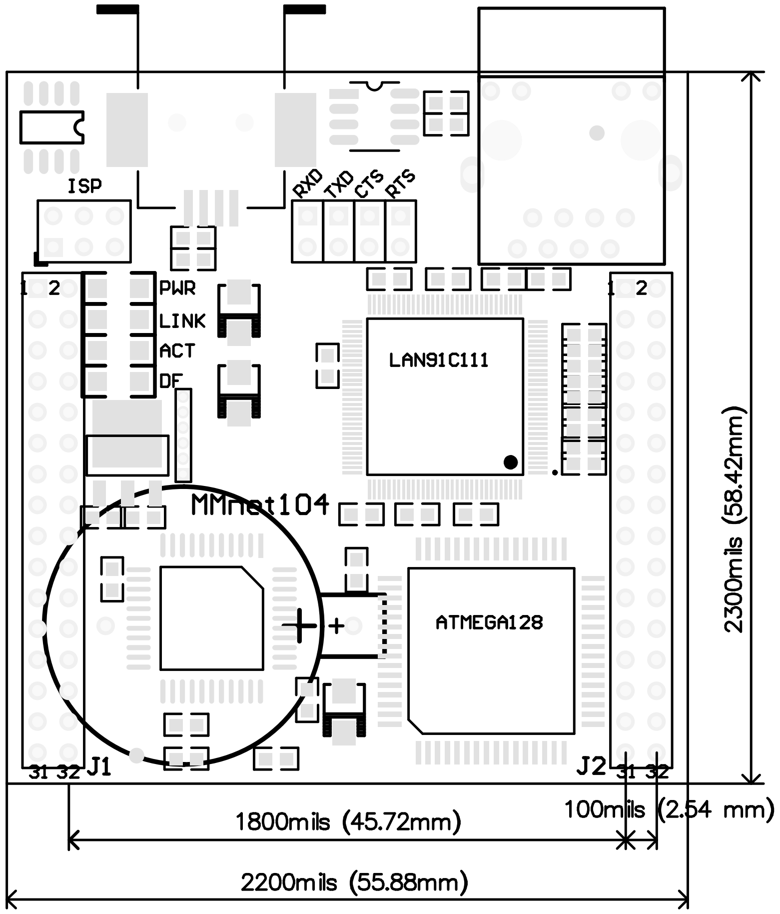


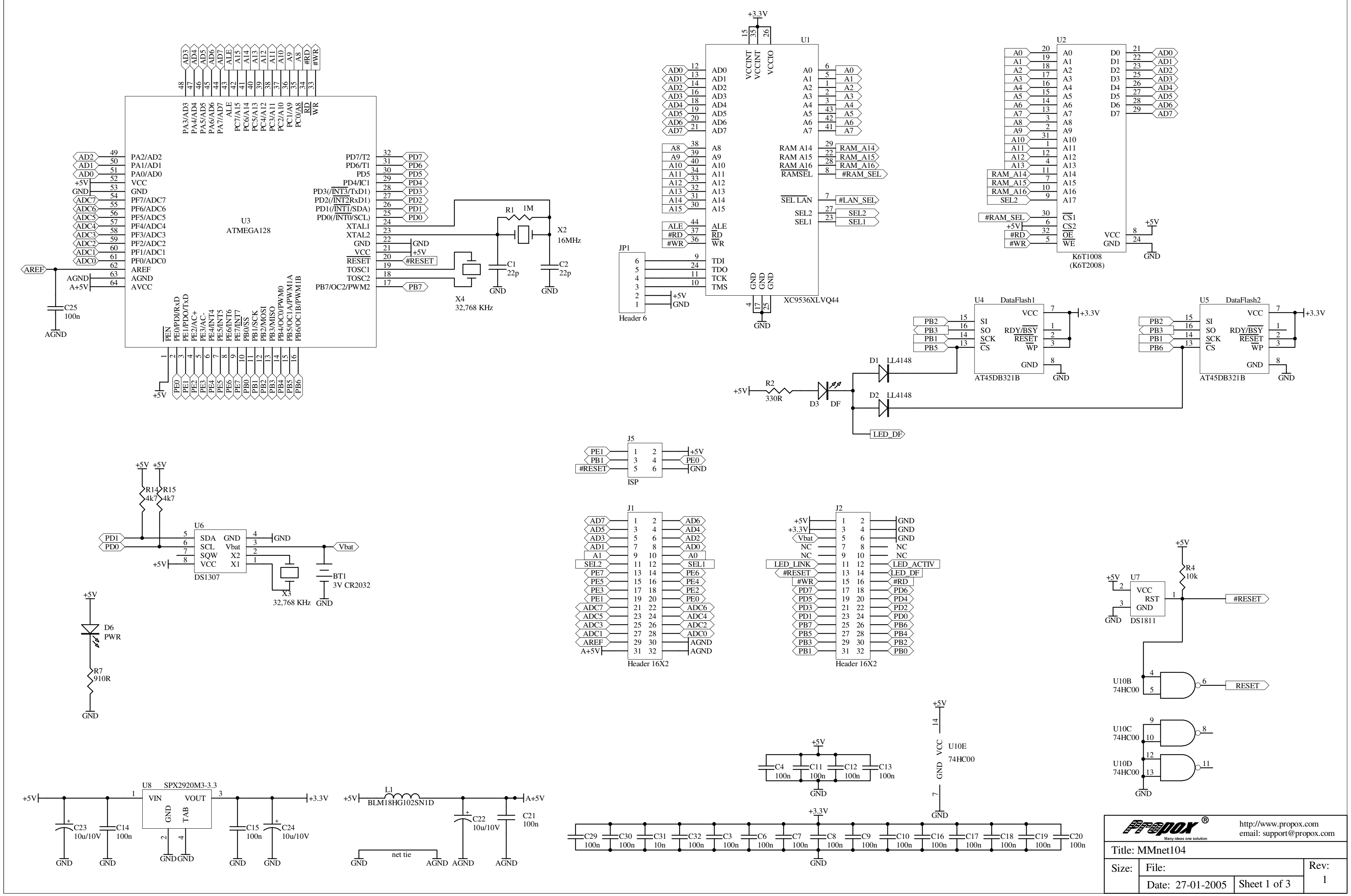
Figure 28 Dimensions – top view.



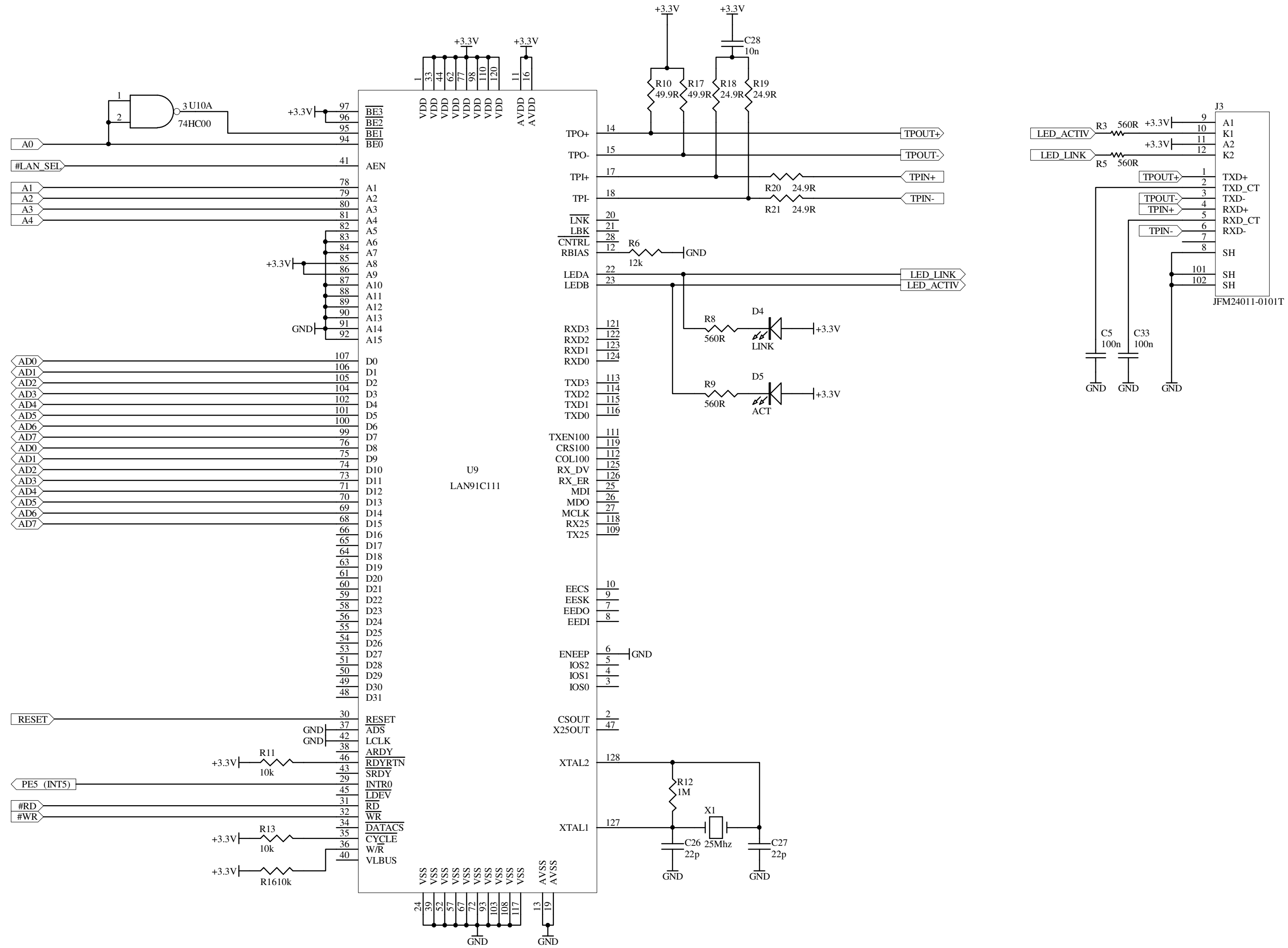
Figure 29 Dimensions – side view.

12 Schematics

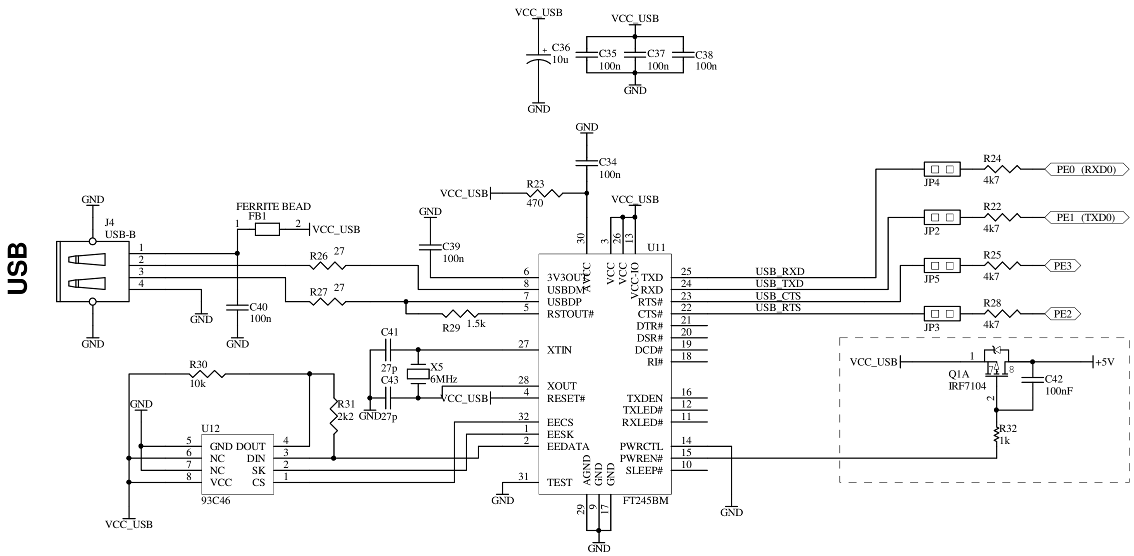
CPU, RAM, DataFlash, RTC



LAN



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Title: MMnet104			
Size:	File:		Rev: 1
	Date: 27-01-2005	Sheet 2 of 3	



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Title: MMnet104		
Size:	File:	Rev: 1
	Date: 27-01-2005	Sheet 3 of 3